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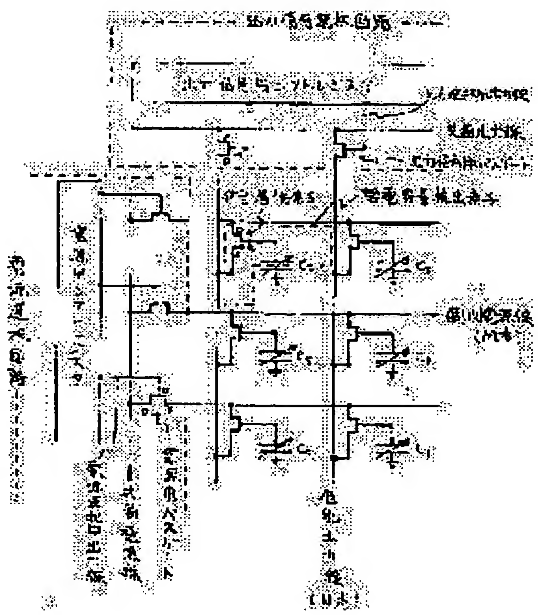
(54) ELECTROSTATIC CAPACITY DETECTOR

(57)Abstract:
PROBLEM TO BE SOLVED: To realize an excellent electrostatic capacity detector.
SOLUTION: This detector is provided with M lines of individual electric power source wires arranged matrix-likely in M rows and N columns, N lines of individual output lines, and electrostatic capacity detecting elements provided in intersections thereof, the each electrostatic capacity detecting element includes a signal detecting element and a signal amplifying element, the signal detecting element includes an electrostatic capacity detecting electrode and an signal detecting dielectric film, and the signal amplifying element consists of a signal amplifying MIS type thin-film semi-conductor device comprising a gate electrode, a gate insulating film and a semi-conductor film.



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CLAIMS

[Claim(s)]

[Claim 1] Electrostatic-capacity detection equipment which depends on detecting electrostatic capacity which is characterized by providing the following, and which changes according to distance with an object, and reads the shape of surface type of this object This electrostatic-capacity detection equipment is M individual power supply lines arranged in the shape of [of a M line N train] a matrix. An electrostatic-capacity sensing element prepared in an intersection of an individual output line of N book, and a this individual power supply line and this individual output line is provided, in this electrostatic-capacity sensing element, this signal sensing element contains a capacity detection electrode and a capacity detection dielectric film including a signal sensing element and a signal amplifier, and this signal amplifier is a gate electrode, a gate insulator layer, and a semiconductor film.

[Claim 2] It is electrostatic-capacity detection equipment according to claim 1 characterized by connecting a source field of said MIS mold thin film semiconductor device for signal amplification to said individual output line, connecting a drain field of said MIS mold thin film semiconductor device for signal amplification to said individual power supply line, and connecting said gate electrode for signal amplification to said capacity detection electrode.

[Claim 3] Gate electrode length of said MIS mold thin film semiconductor device for signal amplification L (micrometer), Thickness of W (micrometer) and a gate insulator layer for gate electrode width of face tox (micrometer), CT=epsilon 0 and epsilonox-L-W/tox define transistor capacity CT of said MIS mold thin film semiconductor device for signal amplification by setting specific inductive capacity of a gate insulator layer to epsilonox (epsilon 0 is a vacuous dielectric constant). Thickness of S (micrometer2) and said capacity detection dielectric film for area of said capacity detection electrode tD (micrometer), It is electrostatic-capacity detection equipment according to claim 2 characterized by vacuous dielectric constant) and this element capacity CD of (epsilon0 being fully larger than this transistor capacity CT when element capacity CD of said signal sensing element was defined as CD=epsilon 0 and epsilonD-S/tD by setting specific inductive capacity of said capacity detection dielectric film to epsilonD.

[Claim 4] Said capacity detection dielectric film is electrostatic-capacity detection equipment according to claim 2 characterized by being located in the maximum front face of said electrostatic-capacity detection

equipment.

[Claim 5] said object -- said capacity detection dielectric film -- touching -- ** -- a ** -- object distance tA -- with, electrostatic-capacity detection equipment according to claim 4 characterized by said transistor capacity CT being fully larger than this object capacity CA when it is separated and object capacity CA is defined as CA=epsilon 0 and epsilonA-S/tA using a vacuous dielectric constant epsilon 0, specific-inductive-capacity epsilonA of air, and area S of said capacity detection electrode.

[Claim 6] Said capacity detection dielectric film is located in the maximum front face of said electrostatic-capacity detection equipment. Gate electrode length of said MIS mold thin film semiconductor device for signal amplification L (micrometer), Thickness of W (micrometer) and a gate insulator layer for gate electrode width of face tox (micrometer), CT=epsilon 0 and epsilonox-L-W/tox define transistor capacity CT of said MIS mold thin film semiconductor device for signal amplification by setting specific inductive capacity of a gate insulator layer to epsilonox (epsilon 0 is a vacuous dielectric constant). Thickness of S (micrometer2) and said capacity detection dielectric film for area of said capacity detection electrode tD (micrometer), When element capacity CD of said signal sensing element is defined as CD=epsilon 0 and epsilonD-S/tD by setting specific inductive capacity of said capacity detection dielectric film to epsilonD, (epsilon0 Vacuous dielectric constant), With, separated this element capacity CD -- this transistor capacity CT -- enough -- large -- said object -- said capacity detection dielectric film -- touching -- ** -- a ** -- object distance tA -- It is electrostatic-capacity detection equipment according to claim 2 characterized by this transistor capacity CT being fully larger than this object capacity CA when object capacity CA is defined as CA=epsilon 0 and epsilonA-S/tA using a vacuous dielectric constant epsilon 0, specific-inductive-capacity epsilonA of air, and area S of said capacity detection electrode.

[Claim 7] Electrostatic-capacity detection equipment which depends on detecting electrostatic capacity which is characterized by providing the following, and which changes according to distance with an object, and reads the shape of surface type of this object This electrostatic-capacity detection equipment is M individual power supply lines arranged in the shape of [of a M line N train] a matrix. An electrostatic-capacity sensing element prepared in an intersection of an individual output line of N book, and a this individual power supply line and this

individual output line and a power supply selection circuitry linked to an individual power supply line of these M books are provided, in this electrostatic-capacity sensing element, this power supply selection circuitry includes a common power supply line and the pass gate for power supplies including a capacity detection electrode, a capacity detection dielectric film, and a signal amplifier, and this signal amplifier is a gate electrode, a gate insulator layer, and a semiconductor film.

[Claim 8] A source field of said MIS mold thin film semiconductor device for signal amplifiers is connected to said individual output line. A drain field of said MIS mold thin film semiconductor device for signal amplifiers is connected to said individual power supply line. A gate electrode of said MIS mold thin film semiconductor device for signal amplifiers is connected to said capacity detection electrode. It is electrostatic-capacity detection equipment according to claim 7 characterized by connecting a source field of said MIS mold thin film semiconductor device for the power supply pass gates to said individual power supply line, and connecting a drain field of said MIS mold thin film semiconductor device for the power supply pass gates to said common power supply line.

[Claim 9] A gate electrode of said MIS mold thin film semiconductor device for the power supply pass gates is electrostatic-capacity detection equipment according to claim 8 characterized by connecting with an output line for power supply selection.

[Claim 10] Said individual output line and said output line for power supply selection are electrostatic-capacity detection equipment according to claim 9 for which said individual power supply line and said common power supply line are wired with the second wiring and which it wires with the first wiring, and is characterized by separating this first wiring and this second wiring electrically through an insulator layer.

[Claim 11] Electrostatic-capacity detection equipment according to claim 10 characterized by wiring said capacity detection electrode with the first wiring.

[Claim 12] Electrostatic-capacity detection equipment according to claim 10 characterized by wiring said capacity detection electrode with the second wiring.

[Claim 13] Electrostatic-capacity detection equipment which depends on detecting electrostatic capacity which is characterized by providing the following, and which changes according to distance with an object, and reads the shape of surface type of this object This electrostatic-capacity detection equipment is M individual power supply lines arranged in the shape of [of a M line N train] a matrix. An

electrostatic-capacity sensing element prepared in an intersection of an individual output line of N book, and a this individual power supply line and this individual output line and an output signal selection circuitry linked to an individual output line of this N book are provided, in this electrostatic-capacity sensing element, this output signal selection circuitry includes a common output line and the pass gate for output signals including a capacity detection electrode, a capacity detection dielectric film, and a signal amplifier, and this signal amplifier is a gate electrode, a gate insulator layer, and a semiconductor film.

[Claim 14] A source field of said MIS mold thin film semiconductor device for signal amplifiers is connected to said individual output line. A drain field of said MIS mold thin film semiconductor device for signal amplifiers is connected to said individual power supply line. A gate electrode of said MIS mold thin film semiconductor device for signal amplifiers is connected to said capacity detection electrode. It is electrostatic-capacity detection equipment according to claim 13 characterized by connecting a source field of said MIS mold thin film semiconductor device for the output signal pass gates to said common output line, and connecting a drain field of said MIS mold thin film semiconductor device for the output signal pass gates to said individual output line.

[Claim 15] A gate electrode of said MIS mold thin film semiconductor device for the output signal pass gates is electrostatic-capacity detection equipment according to claim 14 characterized by connecting with an output line for output selections.

[Claim 16] Said individual output line and said common output line are electrostatic-capacity detection equipment according to claim 15 for which said individual power supply line and said output line for output selections are wired with the second wiring and which it wires with the first wiring, and is characterized by separating this first wiring and this second wiring electrically through an insulator layer.

[Claim 17] Electrostatic-capacity detection equipment according to claim 16 characterized by wiring said capacity detection electrode with the first wiring.

[Claim 18] Electrostatic-capacity detection equipment according to claim 16 characterized by wiring said capacity detection electrode with the second wiring.

[Claim 19] Electrostatic-capacity detection equipment which depends on detecting electrostatic capacity which is characterized by providing the following, and which changes according to distance with an object, and reads the shape of surface type of this object This electrostatic-capacity detection

equipment is M individual power supply lines arranged in the shape of [of a M line N train] a matrix. An electrostatic-capacity sensing element prepared in an intersection of an individual output line of N book, and a this individual power supply line and this individual output line, A power supply selection circuitry linked to an individual power supply line of these M books and an output signal selection circuitry linked to an individual output line of this N book are provided. In this power supply selection circuitry, this output signal selection circuitry includes [this electrostatic-capacity sensing element] a common output line and the pass gate for output signals including a common power supply line and the pass gate for power supplies including a capacity detection electrode, a capacity detection dielectric film, and a signal amplifier, and this signal amplifier is a gate electrode, a gate insulator layer, and a semiconductor film.

[Claim 20] A source field of said MIS mold thin film semiconductor device for signal amplifiers is connected to said individual output line. A drain field of said MIS mold thin film semiconductor device for signal amplifiers is connected to said individual power supply line. A gate electrode of said MIS mold thin film semiconductor device for signal amplifiers is connected to said capacity detection electrode. A source field of said MIS mold thin film semiconductor device for the power supply pass gates is connected to said individual power supply line. A drain field of said MIS mold thin film semiconductor device for the power supply pass gates is connected to said common power supply line. It is electrostatic-capacity detection equipment according to claim 19 characterized by connecting a source field of said MIS mold thin film semiconductor device for the output signal pass gates to said common output line, and connecting a drain field of said MIS mold thin film semiconductor device for the output signal pass gates to said individual output line.

[Claim 21] It is electrostatic-capacity detection equipment according to claim 20 characterized by connecting a gate electrode of said MIS mold thin film semiconductor device for the power supply pass gates to an output line for power supply selection, and connecting a gate electrode of said MIS mold thin film semiconductor device for the output signal pass gates to an output line for output selections.

[Claim 22] Said individual output line and said common output line, and said output line for power supply selection are electrostatic-capacity detection equipment according to claim 21 for which said individual power supply line and said common power supply line, and said output line for output selections are wired with the second wiring and which

it wires with the first wiring, and is characterized by separating this first wiring and this second wiring electrically through an insulator layer.

[Claim 23] Electrostatic-capacity detection equipment according to claim 22 characterized by wiring said capacity detection electrode with the first wiring.

[Claim 24] Electrostatic-capacity detection equipment according to claim 22 characterized by wiring said capacity detection electrode with the second wiring.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[The technical field to which invention belongs] This invention relates to the electrostatic-capacity detection equipment which depends on detecting the electrostatic capacity which changes the shape of surface type of the object which has detailed irregularity, such as a fingerprint, according to the distance on the front face of an object, and is read.

[0002]

[Description of the Prior Art] Conventionally, the electrostatic-capacity detection equipment used for a fingerprint sensor etc. formed in the single crystal silicon substrate the dielectric film prepared on the sensor electrode and the sensor electrode concerned (JP,11-118415,A, JP,2000-346608,A, JP,2001-56204,A, JP,2001-133213,A, etc.). Drawing 1 explains the principle of operation of conventional electrostatic-capacity detection equipment. A sensor electrode and a dielectric film accomplish one electrode and dielectric film of a capacitor, and it changes with the electrode of another side where the body was grounded. The electrostatic capacity CF of this capacitor changes according to the irregularity of the fingerprint which touched the dielectric film front face. On the other hand, the capacitor which accomplishes electrostatic capacity CS is prepared for a semiconductor substrate, the series connection of the two capacitors, such as **, is carried out, and the seal of approval of the predetermined voltage is carried out. Between two capacitors, the charge Q according to the irregularity of a fingerprint is generated by ****(ing). This charge Q was detected using the usual semiconductor technology, and the shape of surface type of an object was read.

[0003]

[Problem(s) to be Solved by the Invention] However, since the equipment concerned was formed on a single crystal silicon substrate, when the conventional electrostatic-capacity detection equipments, such as **, were used as a fingerprint sensor and they forced a finger strongly, they have a technical problem that the equipment concerned

breaks and keeps, and were.

[0004] Furthermore, inevitably [a fingerprint sensor] from the use, about [20mmx20mm] magnitude is called for and the great portion of electrostatic-capacity detection equipment area is occupied with a sensor electrode. Although a sensor electrode is made on a single crystal silicon substrate of course, most single crystal silicon substrates (sensor electrode lower part) which spent huge energy and a huge effort and were created are playing only a role of a mere base material. That is, only by being expensive, there is no conventional electrostatic-capacity detection equipment, and it has a technical problem that it is formed after wasting with great futility.

[0005] in addition, on cards, such as a credit card and an ATM card, a personal authentication function should be prepared and the safety of a card should be raised in recent years -- ** -- indication is strong. since flexibility is missing, the appropriate electrostatic-capacity detection equipment which was alike and was made on the conventional single crystal silicon substrate has the technical problem that the equipment concerned cannot be created on a plastic plate.

[0006] Then, the place made into the object is in view of many situations above-mentioned [this invention] to offer the superior electrostatic-capacity detection equipment which operates to stability, and can reduce still more unnecessary energy and efforts at the time of manufacture, and can be created besides a single crystal silicon substrate.

[0007]

[Means for Solving the Problem] M individual power supply lines by which electrostatic-capacity detection equipment has been arranged in the shape of [of a M line N train] a matrix in electrostatic-capacity detection equipment which depends on this invention detecting electrostatic capacity which changes according to distance with an object, and reads the shape of surface type of an object, An electrostatic-capacity sensing element prepared in an intersection of an individual output line of N book, and an individual power supply line and an individual output line is provided. This electrostatic-capacity sensing element is characterized by a signal amplifier consisting of an MIS mold thin film semiconductor device for signal amplification with which a signal sensing element consists of a gate electrode, a gate insulator layer, and a semiconductor film including a capacity detection electrode and a capacity detection dielectric film including a signal sensing element and a signal amplifier. Furthermore, it succeeds also in a source field of an MIS mold thin film semiconductor device for signal amplification being connected to an

individual output line, a drain field of an MIS mold thin film semiconductor device for signal amplification being connected to an individual power supply line, and a gate electrode for signal amplification being connected to a capacity detection electrode with the feature. Gate electrode length of an MIS mold thin film semiconductor device for signal amplification Moreover, L (micrometer), Thickness of W (micrometer) and a gate insulator layer for gate electrode width of face tox (micrometer), CT=epsilon 0 and epsilonox-L-W/tox define the transistor capacity CT of an MIS mold thin film semiconductor device for signal amplification by setting specific inductive capacity of a gate insulator layer to epsilonox (epsilon 0 is a vacuous dielectric constant). Thickness of S (micrometer2) and a capacity detection dielectric film for area of a capacity detection electrode tD (micrometer), When the element capacity CD of a signal sensing element is defined as CD=epsilon 0 and epsilonD-S/tD by setting specific inductive capacity of a capacity detection dielectric film to epsilonD, (epsilon0 is characterized by vacuous dielectric constant) and this element capacity CD being fully larger than the previous transistor capacity CT. Since a difference of about 10 or more times is generally meant as large enough, if it puts in another way, the element capacity CD and the transistor capacity CT will fill relation with CD>10xCT. It is desirable to locate a capacity detection dielectric film in the maximum front face of electrostatic-capacity detection equipment with electrostatic-capacity detection equipment of this invention. an object -- a capacity detection dielectric film -- touching -- ** -- a ** -- the object distance tA -- with, when it is separated from a capacity detection dielectric film and the object capacity CA is defined as CA=epsilon 0 and epsilonA-S/tA using the vacuous dielectric constant epsilon 0, specific-inductive-capacity epsilonA of air, and the area S of a capacity detection electrode, the previous transistor capacity CT changes more greatly enough than this object capacity CA -- as -- electrostatic-capacity detection equipment -- configuration attachment **. Since it can say that it is large enough in a difference of about 10 or more times being accepted like the above-mentioned, it succeeds in the transistor capacity CT and the object capacity CA filling relation with CT>10xCA with the feature. A capacity detection dielectric film is more ideally located in the maximum front face of electrostatic-capacity detection equipment. L (micrometer) and gate electrode width of face for gate electrode length of an MIS mold thin film semiconductor device for signal amplification W (micrometer), CT=epsilon 0 and epsilonox-L-W/tox define the transistor capacity CT of an

MIS mold thin film semiconductor device for signal amplification, using specific inductive capacity of tox (micrometer) and a gate insulator layer as epsilonox for thickness of a gate insulator layer (epsilon 0 is a vacuous dielectric constant). Thickness of S (micrometer2) and a capacity detection dielectric film for capacity detection electrode area tD (micrometer), When the element capacity CD of a signal sensing element is defined as CD=epsilon 0 and epsilonD-S/tD by setting specific inductive capacity of a capacity detection dielectric film to epsilonD, (epsilon0 Vacuous dielectric constant), With, separated the element capacity CD -- the transistor capacity CT -- enough -- large -- further -- an object -- a capacity detection dielectric film -- touching -- ** -- a ** -- the object distance tA -- When the object capacity CA is defined as CA=epsilon 0 and epsilonA-S/tA using the vacuous dielectric constant epsilon 0, specific-inductive-capacity epsilonA of air, and the capacity detection electrode area S, the transistor capacity CT is more fully than the object capacity CA configuration attachment ** about electrostatic-capacity detection equipment to Mr. large ******. It succeeds in electrostatic-capacity detection equipment with which the element capacity CD, the transistor capacity CT, and the object capacity CA more specifically fill relation with CD>10xCT>100xCA with the feature.

[0008] M individual power supply lines by which electrostatic-capacity detection equipment has been arranged in the shape of [of a M line N train] a matrix in electrostatic-capacity detection equipment which depends on this invention detecting electrostatic capacity which changes according to distance with an object, and reads the shape of surface type of an object, An electrostatic-capacity sensing element prepared in an intersection of an individual output line of N book, and an individual power supply line and an individual output line, Furthermore, provide a power supply selection circuitry linked to M individual power supply lines, and an electrostatic-capacity sensing element contains a capacity detection electrode, a capacity detection dielectric film, and a signal amplifier. A power supply selection circuitry consists of an MIS mold thin film semiconductor device for signal amplification with which a signal amplifier consists of a gate electrode, a gate insulator layer, and a semiconductor film including a common power supply line and the pass gate for power supplies. It is characterized by the pass gate for power supplies consisting of an MIS mold thin film semiconductor device for the power supply pass gates which consists of a gate electrode, a gate insulator layer, and a semiconductor film. In this case, a source field of an MIS mold

thin film semiconductor device for signal amplifiers is connected to an individual output line. A drain field of an MIS mold thin film semiconductor device for signal amplifiers is connected to an individual power supply line. A gate electrode of an MIS mold thin film semiconductor device for signal amplifiers is connected to a capacity detection electrode. It succeeds also in a source field of an MIS mold thin film semiconductor device for the power supply pass gates being connected to an individual power supply line, and a drain field of an MIS mold thin film semiconductor device for the power supply pass gates being connected to a common power supply line with the feature. Moreover, a gate electrode of an MIS mold thin film semiconductor device for the power supply pass gates is connected to an output line for power supply selection which supplies a signal referred to as which individual power supply line to choose from from among M individual power supply lines. With electrostatic-capacity detection equipment of this invention, an individual output line and an output line for power supply selection are wired with the first wiring, an individual power supply line and a common power supply line are wired with the second wiring, and the first wiring, such as **, and the second wiring are electrically separated through an insulator layer. A capacity detection electrode is wired with the first wiring, or is wired with the second wiring.

[0009] M individual power supply lines by which electrostatic-capacity detection equipment has been arranged in the shape of [of a M line N train] a matrix in electrostatic-capacity detection equipment which depends on this invention detecting electrostatic capacity which changes according to distance with an object, and reads the shape of surface type of an object, An electrostatic-capacity sensing element prepared in an intersection of an individual output line of N book, and an individual power supply line and an individual output line, Furthermore, provide an output signal selection circuitry linked to an individual output line of N book, and an electrostatic-capacity sensing element contains a capacity detection electrode, a capacity detection dielectric film, and a signal amplifier. An output signal selection circuitry consists of an MIS mold thin film semiconductor device for signal amplification with which a signal amplifier consists of a gate electrode, a gate insulator layer, and a semiconductor film including a common output line and the pass gate for output signals. It is characterized by the pass gate for output signals consisting of an MIS mold thin film semiconductor device for the output signal pass gates which consists of a gate electrode, a gate insulator layer, and a semiconductor film. In this case, a source

field of an MIS mold thin film semiconductor device for signal amplifiers is connected to an individual output line. A drain field of an MIS mold thin film semiconductor device for signal amplifiers is connected to an individual power supply line. A gate electrode of an MIS mold thin film semiconductor device for signal amplifiers is connected to a capacity detection electrode. It succeeds also in a source field of an MIS mold thin film semiconductor device for the output signal pass gates being connected to a common output line, and a drain field of an MIS mold thin film semiconductor device for the output signal pass gates being connected to said individual output line with the feature. Moreover, a gate electrode of an MIS mold thin film semiconductor device for the output signal pass gates is connected to an output line for output selections which supplies a signal referred to as which individual output line to choose from from among individual output lines of N book. With electrostatic-capacity detection equipment of this invention, an individual output line and a common output line are wired with the first wiring, an individual power supply line and an output line for output selections are wired with the second wiring, and the first wiring, such as **, and this second wiring are electrically separated through an insulator layer. A capacity detection electrode is wired with the first wiring, or is wired with the second wiring.

[0010] M individual power supply lines by which electrostatic-capacity detection equipment has been arranged in the shape of [of a M line N train] a matrix in electrostatic-capacity detection equipment which depends on this invention detecting electrostatic capacity which changes according to distance with an object, and reads the shape of surface type of an object, An electrostatic-capacity sensing element prepared in an intersection of an individual output line of N book, and an individual power supply line and an individual output line, and a power supply selection circuitry linked to M more individual power supply lines, Provide an output signal selection circuitry linked to an individual output line of N book, and an electrostatic-capacity sensing element contains a capacity detection electrode, a capacity detection dielectric film, and a signal amplifier. In a power supply selection circuitry, an output signal selection circuitry includes a common output line and the pass gate for output signals including a common power supply line and the pass gate for power supplies. A signal amplifier consists of an MIS mold thin film semiconductor device for signal amplification which consists of a gate electrode, a gate insulator layer, and a semiconductor film. The pass gate for power supplies consists of an MIS mold

thin film semiconductor device for the power supply pass gates which consists of a gate electrode, a gate insulator layer, and a semiconductor film. It is characterized by the pass gate for output signals consisting of an MIS mold thin film semiconductor device for the output signal pass gates which consists of a gate electrode, a gate insulator layer, and a semiconductor film. In this case; a source field of an MIS mold thin film semiconductor device for signal amplifiers is connected to an individual output line. A drain field of an MIS mold thin film semiconductor device for signal amplifiers is connected to an individual power supply line. A gate electrode of an MIS mold thin film semiconductor device for signal amplifiers is connected to a capacity detection electrode. A source field of an MIS mold thin film semiconductor device for the power supply pass gates is connected to an individual power supply line. A drain field of an MIS mold thin film semiconductor device for the power supply pass gates is connected to a common power supply line. It succeeds also in a source field of an MIS mold thin film semiconductor device for the output signal pass gates being connected to a common output line, and a drain field of an MIS mold thin film semiconductor device for the output signal pass gates being connected to an individual output line with the feature. Moreover, a gate electrode of an MIS mold thin film semiconductor device for the power supply pass gates is connected to an output line for power supply selection which supplies a signal referred to as which individual power supply line to choose from from among M individual power supply lines, and the gate electrode of an MIS mold thin film semiconductor device for the output signal pass gates is connected to an output line for output selections which supplies a signal referred to as which individual output line to choose from from among individual output lines of N book. With electrostatic-capacity detection equipment of this invention, an individual output line, a common output line, and an output line for power supply selection are wired with the first wiring, an individual power supply line, a common power supply line, and an output line for output selections are wired with the second wiring, and the first wiring, such as **, and this second wiring are electrically separated through an insulator layer. A capacity detection electrode is wired with the first wiring, or is wired with the second wiring.

[0011]

[Embodiment of the Invention] This invention depends on detecting the electrostatic capacity which changes according to distance with an object, and creates the electrostatic-capacity detection equipment which reads the

shape of surface type of an object with the MIS mold thin film semiconductor device which consists of a metal-insulator layer-semiconductor film. Since a thin film semiconductor device is usually created on a glass substrate, it is known as technology of manufacturing cheaply the semiconductor integrated circuit which requires a large area, and is concretely applied to the liquid crystal display etc. in these days. Therefore, if the electrostatic-capacity detection equipment which is adapted for a fingerprint sensor etc. is created with a thin film semiconductor device, it is not necessary to use the expensive substrate which consumed the great energy called single crystal silicon substrate, and was made, and the equipment concerned can be created cheaply, without wasting a precious earth resource. Moreover, a thin film semiconductor device is applying the imprint technology indicated by JP,11-312811,A and S.Utsunomiya et.al.Society for Information Display p.916 (2000), and since electrostatic-capacity detection equipment is also released from a single crystal silicon substrate since a semiconductor integrated circuit can be created on a plastic plate, and it can form on a plastic plate, it is.

[0012] now, creating the electrostatic-capacity detection equipment which was adapted in the principle of operation of the **** former with a thin film semiconductor device, although shown in drawing 1 -- the technology of the present thin film semiconductor device -- with, it is impossible if it carries out. Although the charge Q by which induction is carried out between two capacitors by which the series connection was carried out can read Charge Q to accuracy if the single crystal silicon LSI technology which enables high-degree-of-accuracy sensing is used since it is very small, transistor characteristics are not excellent like single crystal silicon LSI technology with a thin film semiconductor device, and although the property deflection between thin film semiconductor devices is also large therefore, Charge Q cannot be read precisely. Then, the electrostatic-capacity detection equipment of this invention makes the electrostatic-capacity sensing element prepared in the intersection of the individual output line of N book (N is one or more integers), and an individual power supply line and an individual output line provide, and this electrostatic-capacity sensing element is considered as a configuration that a signal sensing element and a signal amplifier are included. [M individual power supply lines (M is one or more integers) arranged in the shape of / of a M line N train / a matrix, and] In a capacity detection electrode, Charge Q generates a signal sensing element according to electrostatic capacity including a capacity

detection electrode and a capacity detection dielectric film. In this invention, this charge Q is amplified in the signal amplifier in which it was prepared by each electrostatic-capacity sensing element, and is transformed into current. A signal amplifier consists of the MIS mold thin film semiconductor device for signal amplification which consists of a gate electrode, a gate insulator layer, and a semiconductor film, and, specifically, the gate electrode of the MIS mold thin film semiconductor device for signal amplification is connected to a capacity detection electrode. Principle-of-operation drawing of the invention in this application is shown in drawing 2 . The charge generated between the capacitor with electrostatic capacity Cs and the capacitor which has the electrostatic capacity CF which changes according to the shape of surface type of an object changes the gate potential of the MIS mold thin film semiconductor device for signal amplification. If it **** and the seal of approval of the predetermined voltage is carried out to the drain field of this thin film semiconductor device, the current I which flows between the source drains of a thin film semiconductor device according to the charge Q by which induction was carried out will be amplified remarkably. Since the charge Q itself by which induction was carried out is saved without flowing anywhere, drain voltage is made high, or measurement of Current I also becomes easy by lengthening the measuring time etc., therefore even if it uses a thin film semiconductor device, the shape of surface type of an object can be enough measured to accuracy.

[0013] By the invention in this application, the MIS mold thin film semiconductor device for signal amplification is used as a signal amplifier like the above-mentioned. In this case, a capacitor with electrostatic capacity Cs can be made to serve a double purpose with the MIS mold thin film semiconductor device for signal amplification itself. That is, since new electrostatic capacity replaced with electrostatic capacity Cs is made into the transistor capacity CT of the MIS mold thin film semiconductor device for signal amplification, it is. The capacitor which has electrostatic capacity Cs from an electrostatic-capacity sensing element by ****(ing) is omissible, and a manufacturing process also turns that it is easy at the same time structure is simplified. In addition, it can be said that it is effective in a viewpoint that summarizing two power supplies currently drawn on drawing 2 as a common power supply Vdd can also omit the excessive wiring in electrostatic-capacity detection equipment. ** -- the representative circuit schematic about the principle of

operation in a condition [like] is shown in drawing 3 . The capacitor which has the electrostatic capacity CF which changes according to the shape of surface type of an object, and the capacitor which has the transistor capacity CT are connected to a serial. The transistor capacity CT is electrostatic capacity formed between the drain electrode of the MIS mold thin film semiconductor device for signal amplification, and a gate electrode strictly. What is necessary is to carry out the seal of approval of the voltage Vdd to an individual power supply line, and just to take out the current I which changes according to the shape of surface type of an object from an individual output line, after it connected the source field of the MIS mold thin film semiconductor device for signal amplification to the individual output line for realizing the configuration of drawing 3 , and connecting the drain field of the MIS mold thin film semiconductor device for signal amplification to an individual power supply line.

[0014] The structure of the electrostatic-capacity sensing element which embodies invention which ****(ed) is explained using drawing 4 . The MIS mold thin film semiconductor device for signal amplification which accomplishes the signal amplifier of an electrostatic-capacity sensing element makes a semiconductor film and gate insulator layer including a source field, a channel formation field, and a drain field, and the gate electrode the indispensable requirements for a configuration. In the example of a configuration of drawing 4 , the insulator layer between the first passes has covered this MIS mold thin film semiconductor device for signal amplification. The first wiring is connected to the source field of the MIS mold thin film semiconductor device for signal amplification, and the second wiring is connected to a drain electrode. The second interlayer insulation film was prepared between the first wiring and the second wiring, and the first wiring and the second wiring are separated electrically. It connects with the gate electrode of the MIS mold thin film semiconductor device for signal amplification, and the capacity detection electrode which accomplishes the signal sensing element of an electrostatic-capacity sensing element is formed on the second interlayer insulation film. A capacity detection dielectric film covers a capacity detection electrode top, and a capacity detection dielectric film is located in the maximum front face of electrostatic-capacity detection equipment. A capacity detection dielectric film also plays simultaneously the role of the protective coat of electrostatic-capacity detection equipment. In drawing 4 , although the capacity detection electrode is formed by the second wiring, it may form a capacity

detection electrode with the first wiring. If a capacity detection electrode is formed with the first wiring with the configuration of drawing 4 , the film and the second interlayer insulation film which have been indicated to be a capacity detection dielectric film by drawing 4 will turn into a actual capacity detection dielectric film. Moreover, it also becomes possible to create a capacity detection electrode with the first wiring by forming the second wiring on the insulator layer between the first passes, and forming the first wiring on the second interlayer insulation film.

[0015] In order for the MIS mold thin film semiconductor device for signal amplification of the invention in this application to achieve the function of signal amplification effectively with an above-mentioned configuration, the transistor capacity CT of the MIS mold thin film semiconductor device for signal amplification and the element capacity CD of a signal sensing element must be defined appropriately. Next, relation, such as **, is explained using drawing 5 .

[0016] First, the heights of a measurement management object are in contact with the capacity detection dielectric film, and the condition that the object is grounded electrically is considered. Specifically, detection in the condition that the mountain of a fingerprint is in contact with this electrostatic-capacity detection device table side is assumed, using electrostatic-capacity detection equipment as a fingerprint sensor. The transistor capacity CT of the MIS mold thin film semiconductor device for signal amplification is defined as CT=epsilon 0 and epsilonox-L-W/tox, using [the gate electrode length of the MIS mold thin film semiconductor device for signal amplification / L (micrometer) and gate electrode width of face] specific inductive capacity of tox (micrometer) and a gate insulator layer as epsilonox for the thickness of W (micrometer) and a gate insulator layer. There is epsilon 0 with a vacuous dielectric constant here. Furthermore, the element capacity CD of a signal sensing element is defined as CD=epsilon 0 and epsilonD-S/tD, using [the area of a capacity detection electrode] specific inductive capacity of tD (micrometer) and a capacity detection dielectric film as epsilonD for the thickness of S (micrometer2) and a capacity detection dielectric film (epsilon 0 is a vacuous dielectric constant). An object front face serves as an earth electrode of the element capacity CD, and a capacity detection electrode is equivalent to the electrode of another side on both sides of a capacity detection dielectric film. Since the capacity detection electrode is connected to the gate electrode of the MIS mold thin film semiconductor device for signal amplification, it turns to a ** capacitor

and a capacitor with the element capacity CD being connected to a serial in the transistor capacity CT. The seal of approval of the voltage Vdd is carried out to two series capacitors, such as **, (drawing 5 A). The voltage VGT built over the gate electrode of the MIS mold thin film semiconductor device for signal amplification in this condition since seal-of-approval voltage is divided according to electrostatic capacity is [0017].

[Equation 1]

$$V_{GT} = \frac{V_{dd}}{1+C_D/C_T}$$

It becomes. Therefore, it is [0018] when the element capacity CD is larger enough than the transistor capacity CT.

[Equation 2]

$$C_D >> C_T$$

being alike -- gate voltage -- [0019]

[Equation 3]

$$V_{GT} \approx 0$$

It approximates and voltage is hardly built over a gate electrode. Consequently, the MIS mold thin film semiconductor device for signal amplification will be in an OFF state, it reaches to an extreme of Current I, and it becomes small. When the heights of the object equivalent to the mountain of a fingerprint touch electrostatic-capacity detection equipment after all, in order for a signal amplifier to hardly pass current, it is by the reason for having to set up the gate electrode length which constitutes an electrostatic-capacity sensing element, gate electrode width of face, gate insulator layer construction material, gate insulator layer thickness, capacity detection electrode area, capacity detection dielectric film construction material, capacity detection dielectric thickness, etc. so that the element capacity CD may become larger enough than the transistor capacity CT. Generally the difference of about 10 times is meant as "fully large." If it puts in another way, the element capacity CD and the transistor capacity CT should just fill relation with CD>10xCT. In this case, VGT/Vdd becomes about [0.1 or less] and a thin film semiconductor device cannot grow into an ON state. In order to detect the heights of an object certainly, when the heights of an object touch electrostatic-capacity detection equipment, it is important that the MIS mold thin film semiconductor device for signal amplification grows into an OFF state. Therefore, when using a positive supply for supply voltage Vdd, it is desirable that gate voltage uses the enhancement type (no MARIOFU mold) N type transistor to which drain current does not flow near the zero as an MIS mold thin film semiconductor device for signal amplification. More ideally, an N type MIS thin film semiconductor device

for signal amplification with which this minimum gate voltage fills relation with 0<Vmin<0.1xVdd is used by setting to Vmin gate voltage (the minimum gate voltage) from which the drain current in transfer characteristics serves as the minimum value. In using a negative supply reversely at supply voltage Vdd, gate voltage uses the enhancement type (no MARIOFU mold) P type transistor to which drain current does not flow near the zero as an MIS mold thin film semiconductor device for signal amplification. It is using ideally the P type MIS thin film semiconductor device for signal amplification with which minimum gate voltage Vmin of the P type MIS thin film semiconductor device for signal amplification fills the relation of 0.1xVdd<Vmin<0. It depends on ****(ing), and since the heights of an object can be certainly detected with a gestalt that a current value I is dramatically small, it is.

[0020] next, an object -- a capacity detection dielectric film -- touching -- ** -- a ** -- the object distance tA -- with, the condition which is separated from a capacity detection dielectric film is considered. That is, the crevice of a measurement management object is on a capacity detection dielectric film, and it is in the condition that the object is grounded further electrically. When electrostatic-capacity detection equipment is specifically used as a fingerprint sensor, detection in the condition that the valley of a fingerprint is coming to the electrostatic-capacity detection device table side is assumed. It is [like] desirable to locate [which was described also in advance] a capacity detection dielectric film in the maximum front face of electrostatic-capacity detection equipment with the electrostatic-capacity detection equipment of this invention. The representative circuit schematic at this time is shown in drawing 5 B. Since the object front face is not in contact with a capacity detection dielectric film, between a capacity detection dielectric film and an object front face, the new capacitor which used air as the dielectric is formed. ** is named the object capacity CA and it is defined as CA=epsilon 0 and epsilonA-S/tA using the vacuous dielectric constant epsilon 0, specific-inductive-capacity epsilonA of air, and the area S of a capacity detection electrode. In the condition that ****(ed) and the object separated from the capacity detection dielectric film, three capacitors with the transistor capacity CT, the element capacity CD, and the object capacity CA will be connected to a serial, and the seal of approval of the voltage Vdd will be carried out to three capacitors, such as **, (drawing 5 B). The voltage VGV built over the gate electrode of the MIS mold thin film semiconductor device for signal amplification in this condition since seal-of-approval voltage is divided

among three capacitors according to electrostatic capacity is [0021].
[Equation 4]

It becomes. It is [0022] so that drain current may become very small on the other hand, when an object touches electrostatic-capacity detection equipment in this invention.
[Equation 5]
$C_D >> C_T$

Since an electrostatic-capacity sensing element is created and it is in order to fulfill conditions, VGV is [0023] further.
[Equation 6]
$V_{GV} \approx \frac{V_{dd}}{1+ C_A / C_T}$

It approximates. After all, it is [0024] if the transistor capacity CT is fully larger than the object capacity CA.
[Equation 7]

Gate voltage VGV is [0025].
[Equation 8]

It turns that the thing which spread abbreviation etc. on supply voltage Vdd and to do is possible. Consequently, the MIS mold thin film semiconductor device for signal amplification is made with an ON state, it reaches to an extreme of Current I, and it becomes large. When the crevice of the object equivalent to the valley of a fingerprint comes on electrostatic-capacity detection equipment, in order for a signal amplifier to conduct a high current, there is configuration attachment ****** about the gate electrode length which constitutes a signal amplifier, gate electrode width of face, gate insulator layer construction material, gate insulator layer thickness, etc. so that the transistor capacity CT may become larger enough than the object capacity CA. Since it can say that it is large general enough in the difference of about 10 times being accepted as stated previously, the transistor capacity CT and the object capacity CA should just fill relation with CT>10xCA. In this case, VGT/Vdd becomes about [0.91 or more] and a thin film semiconductor device turns into an ON state easily. In order to detect the crevice of an object certainly, when the crevice of an object approaches electrostatic-capacity detection equipment, it is important that the MIS mold thin film semiconductor device for signal amplification grows into an ON state. When using a positive supply for supply voltage Vdd, a **** cage and a thing with the threshold voltage Vth of this transistor smaller than VGV are desirable in an enhancement type (no

MARIOFU mold) N type transistor as an MIS mold thin film semiconductor device for signal amplification. More ideally, an N type MIS thin film semiconductor device for signal amplification which fills relation with 0<Vth<0.91xVdd is used. When using a negative supply reversely at supply voltage Vdd, on a **** cage and an ideal target, a thing with the larger threshold voltage Vth of the P type MIS thin film semiconductor device for signal amplification than VGV is desirable in an enhancement type (no MARIOFU mold) P type transistor as an MIS mold thin film semiconductor device for signal amplification. It is using more ideally the P type MIS thin film semiconductor device for signal amplification which fills the relation of 0.91xVdd<Vth<0. It depends on ****(ing) and the crevice of an object comes to be certainly detected with a gestalt that a current value I is dramatically large.

[0026] When the heights of the object equivalent to the mountain of a fingerprint etc. touch electrostatic-capacity detection equipment after all, a signal amplifier hardly conducts current. When the crevice of the object which is simultaneously equivalent to the valley of a fingerprint etc. approaches electrostatic-capacity detection equipment, in order for a signal amplifier to recognize the irregularity of an object correctly through big current A capacity detection dielectric film is located in the maximum front face of electrostatic-capacity detection equipment in an electrostatic-capacity sensing element. The gate electrode length L (micrometer) and gate electrode width of face W (micrometer) of the MIS mold thin film semiconductor device for signal amplification Thickness tox (micrometer) of a gate insulator layer, specific-inductive-capacity epsilonox of a gate insulator layer, The capacity detection electrode area S (micrometer2), the thickness tD (micrometer) of a capacity detection dielectric film, It is necessary to set up specific-inductive-capacity epsilonD of a capacity detection dielectric film so that the element capacity CD may become larger enough than the transistor capacity CT. and an object -- a capacity detection dielectric film -- touching -- ** -- a ** -- the object distance tA -- with, when separated, the transistor capacity CT can fully say electrostatic-capacity detection equipment that that of configuration attachment ** is ideal to Mr. large ****** from the object capacity CA. Electrostatic-capacity detection equipment is characterized so that the element capacity CD, the transistor capacity CT, and the object capacity CA may more specifically fill relation with CD>10xCT>100xCA. Moreover, when using a positive supply for supply voltage Vdd, it is ideal that using an

enhancement type (no MARIOFU mold) N type transistor as an MIS mold thin film semiconductor device for signal amplification uses the enhancement type N type transistor which the minimum gate voltage of good **** and this N type transistor fills relation with 0<Vmin<0.1xVdd, and its threshold voltage Vth is still smaller than VGV, and is specifically filling relation with 0<Vth<0.91xVdd. When using a negative supply reversely at supply voltage Vdd, it is desirable to use an enhancement type (no MARIOFU mold) P type transistor as an MIS mold thin film semiconductor device for signal amplification, minimum gate voltage Vmin of this P type transistor fills the relation of 0.1xVdd<Vmin<0, its threshold voltage Vth is still larger than VGV, and it is ideal to use the enhancement type P type transistor which is specifically filling the relation of 0.91xVdd<Vth<0.

[0027] Next, the whole electrostatic-capacity detection equipment configuration which depends on this invention is explained using <u>drawing 6</u> . The electrostatic-capacity detection equipment which reads the shape of surface type of an object is using as the minimum component the electrostatic-capacity sensing element prepared in the intersection of the individual output line of N book (N is one or more integers), and an individual power supply line and an individual output line. [M individual power supply lines (M is one or more integers) arranged in the shape of / of a M line N train / a matrix, and] The electrostatic-capacity detection equipment which depends on this invention in addition to ** etc. may also possess one of the power supply selection circuitry linked to M individual power supply lines, and the output signal selection circuitries linked to the individual output line of N book, or both, and may be. An electrostatic-capacity sensing element detects the electrostatic capacity which changes according to distance with an object including a capacity detection electrode, a capacity detection dielectric film, and a signal amplifier. Since the electrostatic-capacity sensing element is arranged in the shape of [of a M line N train] a matrix, a row and column is scanned sequentially, respectively, and the electrostatic-capacity sensing element of a MxN individual must be chosen as suitable sequence, and it must go to read the shape of surface type of an object. A power supply selection circuitry defines by what kind of sequence a power supply is supplied to each electrostatic-capacity sensing element, and it goes to it. It chooses to any of M individual power supply lines current supply of the power supply selection circuitry is carried out by being including a common power supply line and the pass gate for power supplies at least. An output signal selection

circuitry defines whether in contrast with **, the signal detected in what kind of sequence is read from each electrostatic-capacity sensing element. It chooses from any of the individual output line of N book an output signal selection circuitry takes out an output signal by being including a common output line and the pass gate for output signals at least.

[0028] The signal amplifier in an electrostatic-capacity sensing element consists of MIS mold thin film semiconductor devices for signal amplification which consist of a gate electrode, a gate insulator layer, and a semiconductor film. Moreover, the pass gate for power supplies also consists of MIS mold thin film semiconductor devices for the power supply pass gates which consist of a gate electrode, a gate insulator layer, and a semiconductor film, and consists of the MIS mold thin film semiconductor device for the output signal pass gates with which the pass gate for output signals also consists of a gate electrode, a gate insulator layer, and a semiconductor film. In the invention in this application, the source field of the MIS mold thin film semiconductor device for signal amplifiers is connected to an individual output line, the drain field of the MIS mold thin film semiconductor device for signal amplifiers is connected to an individual power supply line, and the gate electrode of the MIS mold thin film semiconductor device for signal amplifiers is connected to a capacity detection electrode. (At drawing 6 , S and a drain field are displayed by D and the gate electrode is displayed for the source field of an MIS mold thin film semiconductor device in G.) **** is carried out, and an individual power supply line and an individual output line intervene the channel formation field which induces the charge Q detected with the capacity detection electrode, and are connected to each other.

[0029] On the other hand, the source field of the MIS mold thin film semiconductor device for the power supply pass gates is connected to an individual power supply line, the drain field of the MIS mold thin film semiconductor device for the power supply pass gates is connected to a common power supply line, and it connects with the output line for power supply selection which supplies the signal referred to as which individual power supply line the gate electrode of the MIS mold thin film semiconductor device for the power supply pass gates chooses from from among M individual power supply lines. Each output stage of the decoder for power supplies which can make the output line for power supply selection with each output stage of the shift register for power supplies as an example, or is replaced with the shift register for power supplies (in the case of drawing 6) can be made. The shift register for power

supplies carries out sequential supply of the selection signal transmitted to M output stages, and goes. moreover, the decoder for power supplies selects a specific output stage from the output stage of M individual according to the input signal to a decoder. It ****, a selection signal is inputted into the M pass gates for power supplies one by one, the flow with M individual power supply lines as electric one by one as a result as a common power supply line is taken, and it goes. Since the drain field of the MIS thin film semiconductor device for signal amplifiers is connected to an individual power supply line, it turns to the signal amplifiers linked to the selected individual power supply line supplying the current according to the shape of surface type of an object to the output line according to each all at once.

[0030] In the invention in this application, the source field of the MIS mold thin film semiconductor device for the output signal pass gates is connected to a common output line, the drain field of the MIS mold thin film semiconductor device for the output signal pass gates is connected to an individual output line, and it connects with the output line for output selections which supplies the signal referred to as which individual output line the gate electrode of the MIS mold thin film semiconductor device for the output signal pass gates chooses from from among the individual output lines of N book. Each output stage of the decoder for output signals which can make the output line for output selections with each output stage of the shift register for output signals as an example, or is replaced with the shift register for output signals (in the case of <u>drawing 6</u>) can be made. The shift register for output signals carries out sequential supply of the selection signal transmitted to the output stage of N individual, and goes. moreover, the decoder for output signals selects a specific output stage from the output stage of M individual according to the input signal to a decoder. It ****, a selection signal is inputted into the pass gate for output signals of N individual timely one by one, the flow with the individual output line of N book as electric one by one as a result as a common output line is taken, and it goes. Since the source field of the MIS mold thin film semiconductor device for signal amplifiers is connected to an individual output line, only the signal amplifier linked to the individual output line uniquely chosen in the output signal selection circuitry among the signal amplifiers of N individual linked to the individual power supply line chosen in the power supply selection circuitry turns to supplying the current according to the shape of surface type of an object to a common output line. It is scanning the individual output line of N book sequentially, and going similarly

hereafter, where one of M individual output lines is chosen, and the signal from the letter electrostatic-capacity sensing element of a matrix of a M line N train is supplied to a common output line in order, and goes.

[0031] In order for electrostatic-capacity detection equipment to function with the configuration which ****(ed), an individual output line, a common output line, and the output line for power supply selection are wired with the first wiring, an individual power supply line, a common power supply line, and the output line for output selections are wired with the second wiring, and the first wiring, such as **, and this second wiring have the need of dissociating electrically through an insulator layer. A capacity detection electrode may be wired with the first wiring, or may be wired with the second wiring. The parasitic capacitance which removes excessive wiring by accomplishing the configuration of having ****(ed), with is produced between each wiring is made to minimize, therefore very small electrostatic capacity is made to detect in high sensitivity.

[0032] ** -- an electrostatic-capacity sensing element [like] may be formed on a plastic plate using the above-mentioned imprint technology. On a plastic, although the fingerprint sensor based on single crystal silicon technology does not break immediately or does not have sufficient magnitude, it is lacking in practicability to a sake. On the other hand, on a plastic plate, the electrostatic-capacity sensing element on the plastic plate which depends on the invention in this application does not have a fear of an electrostatic-capacity sensing element being divided into covering a finger also as an area large enough, and can be used as a fingerprint sensor on a plastic plate. The smart card which specifically has a personal authentication function by the invention in this application is realized. The smart card equipped with the personal authentication function is used with an ATM card (bankcard), a credit card (credit card), an identification card (Identity card), etc., and has the function which was excellent in if it protects in addition, without making individual fingerprint information flow out out of a card after raising security level, such as **, remarkably.

[0033] (Example 1) After manufacturing the electrostatic-capacity detection equipment which consists of a thin film semiconductor device on a glass substrate, this electrostatic-capacity detection equipment was imprinted on the plastic plate using the imprint technology indicated by JP,11-312811,A and S.Utsunomiya et.al.Society for Information Display p.916 (2000), and electrostatic-capacity detection equipment was created on the plastic

plate. Electrostatic-capacity detection equipment consists of electrostatic-capacity sensing elements located in a line in the shape of [of 400 line 400 trains] a matrix. The magnitude of the matrix section is the square of 20.32mm angle.

[0034] A substrate is polyether sulfone (PES) with a thickness of 400 micrometers. All also of the MIS mold thin film semiconductor device for signal amplification, the MIS mold thin film semiconductor device for the output signal pass gates, the MIS mold thin film semiconductor device for the power supply pass gates, the MIS mold thin film semiconductor device that constitutes the shift register for output signals, and the MIS mold thin film semiconductor device which constitutes the shift register for power supplies are made from the thin film transistor which has the same cross-section structure. A thin film transistor is created with the top gate mold shown in drawing 4 at the low-temperature process of 425 degrees C of process maximum temperatures. The thickness is 59nm in the polycrystal silicon thin film with which the semiconductor film was obtained by laser crystallization. Moreover, a gate insulator layer is an oxidation silicon film of 48nm thickness formed by the chemical-vapor-deposition method (CVD method), and a gate electrode consists of a tantalum thin film with a thickness of 400nm. The specific inductive capacity of the oxidation silicon film which accomplishes a gate insulator layer was called for with abbreviation 3.9 by valve flow coefficient measurement. The insulator layer between the first passes and the second interlayer insulation film are oxidation silicon films formed with the CVD method, using tetraethyl OSO silicate (TEOS:Si4 (OCH2CH3)) and oxygen as a source material. The insulator layer between the first passes is thick about 20% or more, and what is thinner than the second interlayer insulation film is more desirable than a gate electrode (this example 400nm). It is because a gate electrode is covered certainly, a short circuit with a gate electrode, the first wiring, or the second wiring is prevented and the second interlayer insulation film can be simultaneously thickened, if it ****. The insulator layer between the first passes was set to 500nm in this example. The second interlayer insulation film has separated the first wiring and a capacity detection electrode. Therefore, for making into min parasitic capacitance produced between the first wiring and a capacity detection electrode, and realizing the electrostatic-capacity detection equipment of whenever [favorable], the dielectric constant of the second interlayer insulation film is small as much as possible, and its thicker possible one is [the thickness] desirable for it. If

the total thickness of the oxidation silicon film by which the laminating was carried out to **** with the CVD method exceeds about 2 micrometers, a crack may arise in an oxide film and lowering of the yield will be brought about. Therefore, the sum of the insulator layer between the first passes and the second interlayer insulation film may be about 2 micrometers or less. The productivity of electrostatic-capacity detection equipment improves by ****(ing). Since the thicker one is desirable, the second interlayer insulation film is made thicker than the insulator layer between the first passes at the appearance described also in advance. The insulator layer between the first passes is thicker than a gate electrode about 20% or more, the second interlayer insulation film is thicker than the insulator layer between the first passes, and about 2 micrometers or less can say that the sum of the insulator layer between the first passes and the second interlayer insulation film is ideal. Thickness of the second interlayer insulation film was set to 1 micrometer in this example. Each of first wiring and second wiring consists of the aluminum of 500nm thickness, and wiring width of face is 5 micrometers. It depended on the first wiring, the output line for power supply selection, the common output line, and the individual output line were formed, and the individual power supply line, the common power supply line, the output line for output selections, and the capacity detection electrode were formed with the second wiring. The gap of an individual power supply line and a capacity detection electrode is 5 micrometers, and the gap of an individual output line and a capacity detection electrode is also 5 micrometers in arrow flare. In this example, the pitch of the matrix which accomplishes electrostatic-capacity detection equipment is set to 50.8 micrometers, and resolution is set to 500dpi (dots per inch). Therefore, a capacity detection electrode serves as 40.8micrometerx40.8micrometer magnitude. The capacity detection dielectric film was formed by the nitriding silicon film with a thickness of 400nm. Since the specific inductive capacity of this nitriding silicon film was abbreviation 7.5, the element capacity CD serves as about 276 fF(s) (FEMUTO farad) from valve flow coefficient measurement. Since the irregularity of a fingerprint is about 40 micrometers when the electrostatic-capacity detection equipment of this example is assumed to be a fingerprint sensor, the object capacity CA when the valley of a fingerprint comes to an electrostatic-capacity detection device table side is calculated with 0.368fF(s). On the other hand, since the gate electrode length L of the MIS thin film semiconductor device for signal

amplification was set to 4 micrometers and gate electrode width of face W was set to 5 micrometers, the transistor capacity CT serves as about 14.4 fF(s). The electrostatic-capacity sensing element which it **** and is shown in this example fills relation with CD>10xCT>100xCA. If supply voltage Vdd is thus set to 3.3V, the voltage VGT by which a seal of approval is carried out to the gate electrode of the MIS thin film semiconductor device for signal amplification when the mountain of a fingerprint touches an electrostatic-capacity detection device table side is set to 0.16V, and when the valley of a fingerprint comes, the voltage VGV by which a seal of approval is carried out to this gate electrode will be set to 3.22V.

[0035] The transfer characteristics of the MIS mold thin film semiconductor device used in this example are shown in drawing 7 . The shift register for output signals and the shift register for power supplies were considered as the CMOS configuration, and the MIS mold thin film semiconductor device for signal amplification, the MIS mold thin film semiconductor device for the power supply pass gates, and the MIS mold thin film semiconductor device for the output signal pass gates were formed with the NMOS transistor. There is minimum gate voltage Vmin of the N type MIS thin film semiconductor device for signal amplification by 0.1V, and it is filling the relation of 0<Vmin<0.1xVdd=0.33V. Moreover, threshold voltage Vth is 1.47V and is filling the relation of arrow flare 0<Vth<0.91xVdd=3.00V. Consequently, when the mountain of a fingerprint touches an electrostatic-capacity detection device table side, it reaches to an extreme of the current value outputted from a signal amplifier with 5.6x10-13A, and it becomes feeble. When the valley of a fingerprint comes reversely, 2.4x10-5A and big current are outputted from a signal amplifier, and it came to detect concavo-convex information, such as a fingerprint, with a sufficient precision.

[0036]

[Effect of the Invention] the technology which has explained in full detail above using the conventional single crystal silicon substrate like -- severalmmx -- although only about several mm small electrostatic-capacity detection equipment was able to form on a plastic plate, if it depends on the invention in this application, creating the electrostatic-capacity detection equipment which has one 100 times [no less than] the area of this on a plus TIKU substrate will be realized, and moreover, it reaches to an extreme of the concavo-convex information on an object, and it could detect to high degree of accuracy. Consequently, an effect that a metaphor makes the security level of a

smart card improve remarkably is accepted. Moreover, only the pole of equipment area part was using the single crystal silicon semiconductor, but the conventional electrostatic-capacity detection equipment using a single crystal silicon substrate had spent immense energy and an immense effort vainly. on the other hand -- the invention in this application -- ** -- it has an effect that waste [like] is eliminated and it is useful to maintenance of earth environment.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] Drawing explaining the principle of operation in the conventional technology.

[Drawing 2] Drawing explaining the principle of operation in the invention in this application.

[Drawing 3] Drawing explaining the principle of operation in the invention in this application.

[Drawing 4] Drawing explaining the element structure of the invention in this application.

[Drawing 5] Drawing explaining the principle of the invention in this application.

[Drawing 6] Drawing explaining the whole invention-in-this-application configuration.

[Drawing 7] Transfer-characteristics drawing of the thin film semiconductor device used in this example.

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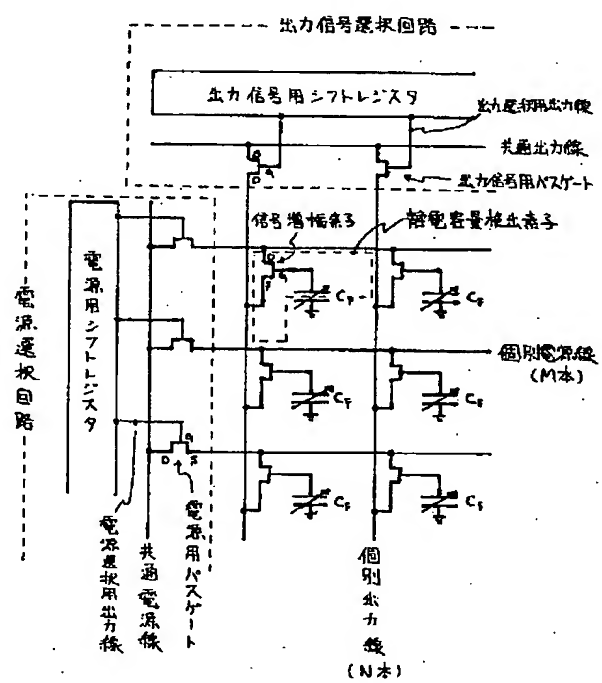
最終頁に続く

(54)【発明の名称】　静電容量検出装置

(57)【要約】

【課題】優良な静電容量検出装置を実現する。

【解決手段】M行N列の行列状に配置されたM本の個別電源線と、N本の個別出力線、及び此等交点に設けられた静電容量検出素子とを具備し、静電容量検出素子は信号検出素子と信号増幅素子とを含み、信号検出素子は容量検出電極と容量検出誘電体膜とを含み、信号増幅素子はゲート電極とゲート絶縁膜と半導体膜とから成る信号増幅用ＭＩＳ型薄膜半導体装置から成る。



【特許請求の範囲】

【請求項１】　対象物との距離に応じて変化する静電容量を検出する事に依り、該対象物の表面形状を読み取る静電容量検出装置に於いて、

該静電容量検出装置はM行N列の行列状に配置されたM本の個別電源線と、N本の個別出力線、及び該個別電源線と該個別出力線との交点に設けられた静電容量検出素子とを具備し、

該静電容量検出素子は信号検出素子と信号増幅素子とを含み、

該信号検出素子は容量検出電極と容量検出誘電体膜とを含み、

該信号増幅素子はゲート電極とゲート絶縁膜と半導体膜とから成る信号増幅用ＭＩＳ型薄膜半導体装置から成る事を特徴とする静電容量検出装置。

【請求項２】　前記信号増幅用ＭＩＳ型薄膜半導体装置のソース領域は前記個別出力線に接続され、

前記信号増幅用ＭＩＳ型薄膜半導体装置のドレイン領域は前記個別電源線に接続され、

前記信号増幅用ゲート電極は前記容量検出電極に接続される事を特徴とした請求項１記載の静電容量検出装置。

【請求項３】　前記信号増幅用ＭＩＳ型薄膜半導体装置のゲート電極長をＬ（μｍ）、ゲート電極幅をＷ（μｍ）、ゲート絶縁膜の厚みをt_{ox}（μｍ）、ゲート絶縁膜の比誘電率をε_{ox}として前記信号増幅用ＭＩＳ型薄膜半導体装置のトランジスタ容量C_Tを

$C_T=\varepsilon_0\cdot\varepsilon_{ox}\cdot L\cdot W/t_{ox}$

にて定義し（ε_0は真空の誘電率）、

前記容量検出電極の面積をＳ（μm^2）、前記容量検出誘電体膜の厚みをt_D（μｍ）、前記容量検出誘電体膜の比誘電率をε_Dとして前記信号検出素子の素子容量C_Dを

$C_D=\varepsilon_0\cdot\varepsilon_D\cdot S/t_D$

と定義した時に（ε_0は真空の誘電率）、

該素子容量C_Dは該トランジスタ容量C_Tよりも十分に大きい事を特徴とした請求項２記載の静電容量検出装置。

【請求項４】　前記容量検出誘電体膜は前記静電容量検出装置の最表面に位置する事を特徴とした請求項２記載の静電容量検出装置。

【請求項５】　前記対象物が前記容量検出誘電体膜に接しずに対象物距離t_Aを以て離れて居り、対象物容量C_Aを真空の誘電率ε_0と空気の比誘電率ε_Aと前記容量検出電極の面積Ｓとを用いて、

$C_A=\varepsilon_0\cdot\varepsilon_A\cdot S/t_A$

と定義した時に、

前記トランジスタ容量C_Tは該対象物容量C_Aよりも十分に大きい事を特徴とする請求項４記載の静電容量検出装置。

【請求項６】　前記容量検出誘電体膜は前記静電容量検出装置の最表面に位置し、

前記信号増幅用ＭＩＳ型薄膜半導体装置のゲート電極長をＬ（μｍ）、ゲート電極幅をＷ（μｍ）、ゲート絶縁膜の厚みをt_{ox}（μｍ）、ゲート絶縁膜の比誘電率をε_{ox}として前記信号増幅用ＭＩＳ型薄膜半導体装置のトランジスタ容量C_Tを

$C_T=\varepsilon_0\cdot\varepsilon_{ox}\cdot L\cdot W/t_{ox}$

にて定義し（ε_0は真空の誘電率）、

前記容量検出電極の面積をＳ（μm^2）、前記容量検出誘電体膜の厚みをt_D（μｍ）、前記容量検出誘電体膜の比誘電率をε_Dとして前記信号検出素子の素子容量C_Dを

$C_D=\varepsilon_0\cdot\varepsilon_D\cdot S/t_D$

と定義した時に（ε_0は真空の誘電率）、

該素子容量C_Dは該トランジスタ容量C_Tよりも十分に大きく、

前記対象物が前記容量検出誘電体膜に接しずに対象物距離t_Aを以て離れて居り、対象物容量C_Aを真空の誘電率ε_0と空気の比誘電率ε_Aと前記容量検出電極の面積Ｓとを用いて、

$C_A=\varepsilon_0\cdot\varepsilon_A\cdot S/t_A$

と定義した時に、

該トランジスタ容量C_Tは該対象物容量C_Aよりも十分に大きい事を特徴とした請求項２記載の静電容量検出装置。

【請求項７】　対象物との距離に応じて変化する静電容量を検出する事に依り、該対象物の表面形状を読み取る静電容量検出装置に於いて、

該静電容量検出装置はM行N列の行列状に配置されたM本の個別電源線と、N本の個別出力線、及び該個別電源線と該個別出力線との交点に設けられた静電容量検出素子、該M本の個別電源線に接続する電源選択回路とを具備し、

該静電容量検出素子は容量検出電極と容量検出誘電体膜と信号増幅素子とを含み、

該電源選択回路は共通電源線と電源用パスゲートとを含み、

該信号増幅素子はゲート電極とゲート絶縁膜と半導体膜とから成る信号増幅用ＭＩＳ型薄膜半導体装置から成り、

該電源用パスゲートはゲート電極とゲート絶縁膜と半導体膜とから成る電源パスゲート用ＭＩＳ型薄膜半導体装置から成る事を特徴とする静電容量検出装置。

【請求項８】　前記信号増幅素子用ＭＩＳ型薄膜半導体装置のソース領域は前記個別出力線に接続され、

前記信号増幅素子用ＭＩＳ型薄膜半導体装置のドレイン領域は前記個別電源線に接続され、

前記信号増幅素子用ＭＩＳ型薄膜半導体装置のゲート電極は前記容量検出電極に接続され、

前記電源パスゲート用ＭＩＳ型薄膜半導体装置のソース

領域は前記個別電源線に接続され、
前記電源パスゲート用ＭＩＳ型薄膜半導体装置のドレイン領域は前記共通電源線に接続される事を特徴とする請求項７記載の静電容量検出装置。
【請求項９】　前記電源パスゲート用ＭＩＳ型薄膜半導体装置のゲート電極は電源選択用出力線に接続される事を特徴とする請求項８記載の静電容量検出装置。
【請求項１０】　前記個別出力線と前記電源選択用出力線とは第一配線にて配線され、
前記個別電源線と前記共通電源線とは第二配線にて配線され、該第一配線と該第二配線とは絶縁膜を介して電気的に分離されて居る事を特徴とする請求項９記載の静電容量検出装置。
【請求項１１】　前記容量検出電極が第一配線にて配線されて居る事を特徴とする請求項１０記載の静電容量検出装置。
【請求項１２】　前記容量検出電極が第二配線にて配線されて居る事を特徴とする請求項１０記載の静電容量検出装置。
【請求項１３】　対象物との距離に応じて変化する静電容量を検出する事に依り、該対象物の表面形状を読み取る静電容量検出装置に於いて、
該静電容量検出装置はM行Ｎ列の行列状に配置されたＭ本の個別電源線と、Ｎ本の個別出力線、及び該個別電源線と該個別出力線との交点に設けられた静電容量検出素子、該Ｎ本の個別出力線に接続する出力信号選択回路とを具備し、
該静電容量検出素子は容量検出電極と容量検出誘電体膜と信号増幅素子とを含み、
該出力信号選択回路は共通出力線と出力信号用パスゲートとを含み、
該信号増幅素子はゲート電極とゲート絶縁膜と半導体膜とから成る信号増幅用ＭＩＳ型薄膜半導体装置から成り、
該出力信号用パスゲートはゲート電極とゲート絶縁膜と半導体膜とから成る出力信号パスゲート用ＭＩＳ型薄膜半導体装置から成る事を特徴とする静電容量検出装置。
【請求項１４】　前記信号増幅素子用ＭＩＳ型薄膜半導体装置のソース領域は前記個別出力線に接続され、
前記信号増幅素子用ＭＩＳ型薄膜半導体装置のドレイン領域は前記個別電源線に接続され、
前記信号増幅素子用ＭＩＳ型薄膜半導体装置のゲート電極は前記容量検出電極に接続され、
前記出力信号パスゲート用ＭＩＳ型薄膜半導体装置のソース領域は前記共通出力線に接続され、
前記出力信号パスゲート用ＭＩＳ型薄膜半導体装置のドレイン領域は前記個別出力線に接続される事を特徴とする請求項１３記載の静電容量検出装置。
【請求項１５】　前記出力信号パスゲート用ＭＩＳ型薄膜半導体装置のゲート電極は出力選択用出力線に接続される事を特徴とする請求項１４記載の静電容量検出装置。

【請求項１６】　前記個別出力線と前記共通出力線とは第一配線にて配線され、
前記個別電源線と前記出力選択用出力線とは第二配線にて配線され、該第一配線と該第二配線とは絶縁膜を介して電気的に分離されて居る事を特徴とする請求項１５記載の静電容量検出装置。
【請求項１７】　前記容量検出電極が第一配線にて配線されて居る事を特徴とする請求項１６記載の静電容量検出装置。
【請求項１８】　前記容量検出電極が第二配線にて配線されて居る事を特徴とする請求項１６記載の静電容量検出装置。
【請求項１９】　対象物との距離に応じて変化する静電容量を検出する事に依り、該対象物の表面形状を読み取る静電容量検出装置に於いて、
該静電容量検出装置はM行Ｎ列の行列状に配置されたＭ本の個別電源線と、Ｎ本の個別出力線、及び該個別電源線と該個別出力線との交点に設けられた静電容量検出素子、該M本の個別電源線に接続する電源選択回路、該Ｎ本の個別出力線に接続する出力信号選択回路とを具備し、
該静電容量検出素子は容量検出電極と容量検出誘電体膜と信号増幅素子とを含み、
該電源選択回路は共通電源線と電源用パスゲートとを含み、
該出力信号選択回路は共通出力線と出力信号用パスゲートとを含み、
該信号増幅素子はゲート電極とゲート絶縁膜と半導体膜とから成る信号増幅用ＭＩＳ型薄膜半導体装置から成り、
該電源用パスゲートはゲート電極とゲート絶縁膜と半導体膜とから成る電源パスゲート用ＭＩＳ型薄膜半導体装置から成り、
該出力信号用パスゲートはゲート電極とゲート絶縁膜と半導体膜とから成る出力信号パスゲート用ＭＩＳ型薄膜半導体装置から成る事を特徴とする静電容量検出装置。
【請求項２０】　前記信号増幅素子用ＭＩＳ型薄膜半導体装置のソース領域は前記個別出力線に接続され、
前記信号増幅素子用ＭＩＳ型薄膜半導体装置のドレイン領域は前記個別電源線に接続され、
前記信号増幅素子用ＭＩＳ型薄膜半導体装置のゲート電極は前記容量検出電極に接続され、
前記電源パスゲート用ＭＩＳ型薄膜半導体装置のソース領域は前記個別電源線に接続され、
前記電源パスゲート用ＭＩＳ型薄膜半導体装置のドレイン領域は前記共通電源線に接続され、
前記出力信号パスゲート用ＭＩＳ型薄膜半導体装置のソース領域は前記共通出力線に接続され、

前記出力信号パスゲート用ＭＩＳ型薄膜半導体装置のドレイン領域は前記個別出力線に接続される事を特徴とする請求項１９記載の静電容量検出装置。

【請求項２１】　前記電源パスゲート用ＭＩＳ型薄膜半導体装置のゲート電極は電源選択用出力線に接続され、前記出力信号パスゲート用ＭＩＳ型薄膜半導体装置のゲート電極は出力選択用出力線に接続される事を特徴とする請求項２０記載の静電容量検出装置。

【請求項２２】　前記個別出力線と前記共通出力線と前記電源選択用出力線とは第一配線にて配線され、
前記個別電源線と前記共通電源線と前記出力選択用出力線とは第二配線にて配線され、該第一配線と該第二配線とは絶縁膜を介して電気的に分離されて居る事を特徴とする請求項２１記載の静電容量検出装置。

【請求項２３】　前記容量検出電極が第一配線にて配線されて居る事を特徴とする請求項２２記載の静電容量検出装置。

【請求項２４】　前記容量検出電極が第二配線にて配線されて居る事を特徴とする請求項２２記載の静電容量検出装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は指紋等の微細な凹凸を有する対象物の表面形状を、対象物表面との距離に応じて変化する静電容量を検出する事に依り読み取る静電容量検出装置に関する。

【０００２】

【従来の技術】従来、指紋センサ等に用いられる静電容量検出装置はセンサ電極と当該センサ電極上に設けられた誘電体膜とを単結晶硅素基板に形成していた（特開平１１－１１８４１５、特開２０００－３４６６０８、特開２００１－５６２０４、特開２００１－１３３２１３等）。図１は従来の静電容量検出装置の動作原理を説明している。センサ電極と誘電体膜とがコンデンサの一方の電極と誘電体膜とを成し、人体が接地された他方の電極と成る。このコンデンサーの静電容量C_Fは誘電体膜表面に接した指紋の凹凸に応じて変化する。一方、半導体基板には静電容量C_Sを成すコンデンサーを準備し、此等二つのコンデンサーを直列接続して、所定の電圧を印可する。斯うする事で二つのコンデンサーの間には指紋の凹凸に応じた電荷Ｑが発生する。この電荷Ｑを通常の半導体技術を用いて検出し、対象物の表面形状を読み取っていた。

【０００３】

【発明が解決しようとする課題】しかしながら此等従来の静電容量検出装置は、当該装置が単結晶硅素基板上に形成されて居る為に、指紋センサとして用いると指を強く押しつけた際に当該装置が割れて仕舞うとの課題を有して居た。

【０００４】更に指紋センサはその用途から必然的に２０ｍｍ×２０ｍｍ程度の大きさが求められ、静電容量検出装置面積の大部分はセンサ電極にて占められる。センサ電極は無論単結晶硅素基板上に作られるが、膨大なエネルギーと労力とを費やして作成された単結晶硅素基板の大部分（センサ電極下部）は単なる支持体としての役割しか演じてない。即ち従来の静電容量検出装置は高価なだけでは無く、多大なる無駄と浪費の上に形成されて居るとの課題を有する。

【０００５】加えて近年、クレジットカードやキャッシュカード等のカード上に個人認証機能を設けてカードの安全性を高めるべきとの指摘が強い。然るに従来の単結晶硅素基板上に作られた静電容量検出装置は柔軟性に欠ける為に、当該装置をプラスティック基板上に作成し得ないとの課題を有している。

【０００６】そこで本発明は上述の諸事情を鑑み、その目的とする所は安定に動作し、更に製造時に不要なエネルギーや労力を削減し得、又単結晶硅素基板以外にも作成し得る優良な静電容量検出装置を提供する事に有る。

【０００７】

【課題を解決するための手段】本発明は対象物との距離に応じて変化する静電容量を検出する事に依り、対象物の表面形状を読み取る静電容量検出装置に於いて、静電容量検出装置はM行N列の行列状に配置されたM本の個別電源線と、Ｎ本の個別出力線、及び個別電源線と個別出力線との交点に設けられた静電容量検出素子とを具備し、此の静電容量検出素子は信号検出素子と信号増幅素子とを含み、信号検出素子は容量検出電極と容量検出誘電体膜とを含み、信号増幅素子はゲート電極とゲート絶縁膜と半導体膜とから成る信号増幅用ＭＩＳ型薄膜半導体装置から成る事を特徴とする。更に信号増幅用ＭＩＳ型薄膜半導体装置のソース領域が個別出力線に接続され、信号増幅用ＭＩＳ型薄膜半導体装置のドレイン領域が個別電源線に接続され、信号増幅用ゲート電極が容量検出電極に接続される事をも特徴と為す。又、信号増幅用ＭＩＳ型薄膜半導体装置のゲート電極長をＬ（μｍ）、ゲート電極幅をＷ（μｍ）、ゲート絶縁膜の厚みをt_{ox}（μｍ）、ゲート絶縁膜の比誘電率をε_{ox}として信号増幅用ＭＩＳ型薄膜半導体装置のトランジスタ容量C_Tを

$$C_T=\varepsilon_0\cdot\varepsilon_{ox}\cdot L\cdot W/t_{ox}$$

にて定義し（ε_0は真空の誘電率）、容量検出電極の面積をＳ（μm^2）、容量検出誘電体膜の厚みをt_D（μｍ）、容量検出誘電体膜の比誘電率をε_Dとして信号検出素子の素子容量C_Dを

$$C_D=\varepsilon_0\cdot\varepsilon_D\cdot S/t_D$$

と定義した時に（ε_0は真空の誘電率）、此の素子容量C_Dは先のトランジスタ容量C_Tよりも十分に大きい事を特徴とする。十分に大きいとは一般的に１０倍程度以上の相違を意味するので、換言すれば素子容量C_Dとトランジスタ容量C_Tとが

$C_D > 10 \times C_T$

との関係を満たしている事になる。本発明の静電容量検出装置では容量検出誘電体膜が静電容量検出装置の最表面に位置するのが望ましい。対象物が容量検出誘電体膜に接しずに対象物距離t_Aを以て容量検出誘電体膜から離れて居り、対象物容量C_Aを真空の誘電率ε_0と空気の比誘電率ε_Aと容量検出電極の面積Ｓとを用いて、

$C_A = \varepsilon_0 \cdot \varepsilon_A \cdot S / t_A$

と定義した時に、先のトランジスタ容量C_Tは此の対象物容量C_Aよりも十分に大きく成る様に静電容量検出装置を構成づける。前述の如く、１０倍程度以上の相違が認められると十分に大きいと言えるので、トランジスタ容量C_Tと対象物容量C_Aとが

$C_T > 10 \times C_A$

との関係を満たしている事を特徴と為す。より理想的には、容量検出誘電体膜が静電容量検出装置の最表面に位置し、信号増幅用ＭＩＳ型薄膜半導体装置のゲート電極長をＬ（μｍ）、ゲート電極幅をＷ（μｍ）、ゲート絶縁膜の厚みをt_{ox}（μｍ）、ゲート絶縁膜の比誘電率をε_{ox}として信号増幅用ＭＩＳ型薄膜半導体装置のトランジスタ容量C_Tを

$C_T = \varepsilon_0 \cdot \varepsilon_{ox} \cdot L \cdot W / t_{ox}$

にて定義し（ε_0は真空の誘電率）、容量検出電極面積をＳ（μm^2）、容量検出誘電体膜の厚みをt_D（μｍ）、容量検出誘電体膜の比誘電率をε_Dとして信号検出素子の素子容量C_Dを

$C_D = \varepsilon_0 \cdot \varepsilon_D \cdot S / t_D$

と定義した時に（ε_0は真空の誘電率）、素子容量C_Dはトランジスタ容量C_Tよりも十分に大きく、更に対象物が容量検出誘電体膜に接しずに対象物距離t_Aを以て離れて居り、対象物容量C_Aを真空の誘電率ε_0と空気の比誘電率ε_Aと容量検出電極面積Ｓとを用いて、

$C_A = \varepsilon_0 \cdot \varepsilon_A \cdot S / t_A$

と定義した時に、トランジスタ容量C_Tが対象物容量C_Aよりも十分に大く成る様に静電容量検出装置を構成づける。より具体的には素子容量C_Dとトランジスタ容量C_Tと対象物容量C_Aとが

$C_D > 10 \times C_T > 100 \times C_A$

との関係を満たす様な静電容量検出装置を特徴と為す。

【０００８】本発明は対象物との距離に応じて変化する静電容量を検出する事に依り、対象物の表面形状を読み取る静電容量検出装置に於いて、静電容量検出装置はＭ行Ｎ列の行列状に配置されたＭ本の個別電源線と、Ｎ本の個別出力線、及び個別電源線と個別出力線との交点に設けられた静電容量検出素子、更にはＭ本の個別電源線に接続する電源選択回路とを具備し、静電容量検出素子は容量検出電極と容量検出誘電体膜と信号増幅素子とを含み、電源選択回路は共通電源線と電源用パスゲートとを含み、信号増幅素子はゲート電極とゲート絶縁膜と半導体膜とから成る信号増幅用ＭＩＳ型薄膜半導体装置から成り、電源用パスゲートはゲート電極とゲート絶縁膜と半導体膜とから成る電源パスゲート用ＭＩＳ型薄膜半導体装置から成る事を特徴とする。この際に信号増幅素子用ＭＩＳ型薄膜半導体装置のソース領域は個別出力線に接続され、信号増幅素子用ＭＩＳ型薄膜半導体装置のドレイン領域は個別電源線に接続され、信号増幅素子用ＭＩＳ型薄膜半導体装置のゲート電極は容量検出電極に接続され、電源パスゲート用ＭＩＳ型薄膜半導体装置のソース領域は個別電源線に接続され、電源パスゲート用ＭＩＳ型薄膜半導体装置のドレイン領域は共通電源線に接続される事をも特徴と為す。又、電源パスゲート用ＭＩＳ型薄膜半導体装置のゲート電極は、Ｍ本の個別電源線の内からどの個別電源線を選択するかと云った信号を供給する電源選択用出力線に接続される。本発明の静電容量検出装置では個別出力線と電源選択用出力線とが第一配線にて配線され、個別電源線と共通電源線とが第二配線にて配線され、此等第一配線と第二配線とは絶縁膜を介して電気的に分離されて居る。容量検出電極は第一配線にて配線されるか、或いは第二配線にて配線される。

【０００９】本発明は対象物との距離に応じて変化する静電容量を検出する事に依り、対象物の表面形状を読み取る静電容量検出装置に於いて、静電容量検出装置はＭ行Ｎ列の行列状に配置されたＭ本の個別電源線と、Ｎ本の個別出力線、及び個別電源線と個別出力線との交点に設けられた静電容量検出素子、更にはＮ本の個別出力線に接続する出力信号選択回路とを具備し、静電容量検出素子は容量検出電極と容量検出誘電体膜と信号増幅素子とを含み、出力信号選択回路は共通出力線と出力信号用パスゲートとを含み、信号増幅素子はゲート電極とゲート絶縁膜と半導体膜とから成る信号増幅用ＭＩＳ型薄膜半導体装置から成り、出力信号用パスゲートはゲート電極とゲート絶縁膜と半導体膜とから成る出力信号パスゲート用ＭＩＳ型薄膜半導体装置から成る事を特徴とする。この際に信号増幅素子用ＭＩＳ型薄膜半導体装置のソース領域は個別出力線に接続され、信号増幅素子用ＭＩＳ型薄膜半導体装置のドレイン領域は個別電源線に接続され、信号増幅素子用ＭＩＳ型薄膜半導体装置のゲート電極は容量検出電極に接続され、出力信号パスゲート用ＭＩＳ型薄膜半導体装置のソース領域は共通出力線に接続され、出力信号パスゲート用ＭＩＳ型薄膜半導体装置のドレイン領域は前記個別出力線に接続される事をも特徴と為す。又、出力信号パスゲート用ＭＩＳ型薄膜半導体装置のゲート電極は、Ｎ本の個別出力線の内からどの個別出力線を選択するかと云った信号を供給する出力選択用出力線に接続される。本発明の静電容量検出装置では個別出力線と共通出力線とが第一配線にて配線され、個別電源線と出力選択用出力線とが第二配線にて配線され、此等第一配線と該第二配線とは絶縁膜を介して電気的に分離されて居る。容量検出電極は第一配線にて

配線されるか、或いは第二配線にて配線される。

【００１０】本発明は対象物との距離に応じて変化する静電容量を検出する事に依り、対象物の表面形状を読み取る静電容量検出装置に於いて、静電容量検出装置はM行N列の行列状に配置されたM本の個別電源線と、N本の個別出力線、及び個別電源線と個別出力線との交点に設けられた静電容量検出素子、更にはM本の個別電源線に接続する電源選択回路と、N本の個別出力線に接続する出力信号選択回路とを具備し、静電容量検出素子は容量検出電極と容量検出誘電体膜と信号増幅素子とを含み、電源選択回路は共通電源線と電源用パスゲートとを含み、出力信号選択回路は共通出力線と出力信号用パスゲートとを含み、信号増幅素子はゲート電極とゲート絶縁膜と半導体膜とから成る信号増幅用ＭＩＳ型薄膜半導体装置から成り、電源用パスゲートはゲート電極とゲート絶縁膜と半導体膜とから成る電源パスゲート用ＭＩＳ型薄膜半導体装置から成り、出力信号用パスゲートはゲート電極とゲート絶縁膜と半導体膜とから成る出力信号パスゲート用ＭＩＳ型薄膜半導体装置から成る事を特徴とする。この際に信号増幅素子用ＭＩＳ型薄膜半導体装置のソース領域は個別出力線に接続され、信号増幅素子用ＭＩＳ型薄膜半導体装置のドレイン領域は個別電源線に接続され、信号増幅素子用ＭＩＳ型薄膜半導体装置のゲート電極は容量検出電極に接続され、電源パスゲート用ＭＩＳ型薄膜半導体装置のソース領域は個別電源線に接続され、電源パスゲート用ＭＩＳ型薄膜半導体装置のドレイン領域は共通電源線に接続され、出力信号パスゲート用ＭＩＳ型薄膜半導体装置のソース領域は共通出力線に接続され、出力信号パスゲート用ＭＩＳ型薄膜半導体装置のドレイン領域は個別出力線に接続される事をも特徴と為す。又、電源パスゲート用ＭＩＳ型薄膜半導体装置のゲート電極は、M本の個別電源線の内からどの個別電源線を選択するかと云った信号を供給する電源選択用出力線に接続され、出力信号パスゲート用ＭＩＳ型薄膜半導体装置のゲート電極は、N本の個別出力線の内からどの個別出力線を選択するかと云った信号を供給する出力選択用出力線に接続される。本発明の静電容量検出装置では個別出力線と共通出力線と電源選択用出力線とが第一配線にて配線され、個別電源線と共通電源線と出力選択用出力線とが第二配線にて配線され、此等第一配線と該第二配線とは絶縁膜を介して電気的に分離されて居る。容量検出電極は第一配線にて配線されるか、或いは第二配線にて配線される。

【００１１】

【発明の実施の形態】本発明は対象物との距離に応じて変化する静電容量を検出する事に依り、対象物の表面形状を読み取る静電容量検出装置を金属－絶縁膜－半導体膜から成るＭＩＳ型薄膜半導体装置にて作成する。薄膜半導体装置は通常硝子基板上に作成される為に、大面積を要する半導体集積回路を安価に製造する技術として知られ、具体的に昨今では液晶表示装置等に応用されている。従って指紋センサ等に適応される静電容量検出装置を薄膜半導体装置にて作成すると、単結晶硅素基板と云った多大なエネルギーを消費して作られた高価な基板を使用する必要がなく、貴重な地球資源を浪費する事なく安価に当該装置を作成し得る。又、薄膜半導体装置は特開平１１－３１２８１１やS. Utsunomiya et. al. Society for Information Display p. 916 (2000)に開示された転写技術を適用する事で、半導体集積回路をプラスティック基板上に作成出来るので、静電容量検出装置も単結晶硅素基板から解放されてプラスティック基板上に形成し得るので有る。

【００１２】さて、図１に示すが如き従来の動作原理を適応した静電容量検出装置を薄膜半導体装置にて作成するのは、現在の薄膜半導体装置の技術を以てしては不可能である。二つの直列接続されたコンデンサー間に誘起される電荷Ｑは非常に小さい為に、高精度感知を可能とする単結晶硅素ＬＳＩ技術を用いれば電荷Ｑを正確に読み取れるが、薄膜半導体装置ではトランジスタ特性が単結晶硅素ＬＳＩ技術程には優れず、又薄膜半導体装置間の特性偏差も大きいが故に電荷Ｑを精確に読み取れない。そこで本発明の静電容量検出装置はM行N列の行列状に配置されたM本（Mは１以上の整数）の個別電源線と、N本（Nは１以上の整数）の個別出力線、及び個別電源線と個別出力線との交点に設けられた静電容量検出素子とを具備せしめ、此の静電容量検出素子は信号検出素子と信号増幅素子とを含むとの構成とする。信号検出素子は容量検出電極と容量検出誘電体膜とを含み、容量検出電極には静電容量に応じて電荷Ｑが発生する。本発明ではこの電荷Ｑを各静電容量検出素子に設けられた信号増幅素子にて増幅し、電流に変換する。具体的には信号増幅素子はゲート電極とゲート絶縁膜と半導体膜とから成る信号増幅用ＭＩＳ型薄膜半導体装置から成り、信号増幅用ＭＩＳ型薄膜半導体装置のゲート電極が容量検出電極に接続される。図２に本願発明の動作原理図を示す。静電容量C_Sを持つコンデンサーと、対象物の表面形状に応じて変化する静電容量C_Fを有するコンデンサーとの間に発生した電荷は信号増幅用ＭＩＳ型薄膜半導体装置のゲート電位を変化させる。斯うして此の薄膜半導体装置のドレイン領域に所定の電圧を印可すると、誘起された電荷Ｑに応じて薄膜半導体装置のソースドレイン間に流れる電流Ｉは著しく増幅される。誘起された電荷Ｑ自体は何処にも流れずに保存されるので、ドレイン電圧を高くしたり或いは測定時間を長くする等で電流Ｉの測定も容易になり、従って薄膜半導体装置を用いても対象物の表面形状を十分正確に計測出来る様になる。

【００１３】前述の如く本願発明では信号増幅素子として信号増幅用ＭＩＳ型薄膜半導体装置を用いて居る。この場合、静電容量C_Sを持つコンデンサーを信号増幅用ＭＩＳ型薄膜半導体装置其の物で兼用し得る。即ち静電

容量C_sに代わる新たな静電容量を信号増幅用ＭＩＳ型薄膜半導体装置のトランジスタ容量C_Tとするので有る。斯うする事で静電容量検出素子から静電容量C_sを持つコンデンサーを省略出来、構造が簡素化されると同時に製造工程も容易と化す。加えて図２に描かれて居る二つの電源を共通の電源V_{dd}として纏める事も静電容量検出装置内に於ける余計な配線を省略し得るとの観点で効果的と言える。斯様な状態に於ける動作原理に関する等価回路図を図３に示す。対象物の表面形状に応じて変化する静電容量C_Fを有するコンデンサーとトランジスタ容量C_Tを有するコンデンサーとが直列に接続されて居る。厳密にはトランジスタ容量C_Tは信号増幅用ＭＩＳ型薄膜半導体装置のドレイン電極とゲート電極との間に形成される静電容量である。図３の構成を実現させるには信号増幅用ＭＩＳ型薄膜半導体装置のソース領域を個別出力線に接続し、信号増幅用ＭＩＳ型薄膜半導体装置のドレイン領域を個別電源線に接続した上で、個別電源線に電圧V_{dd}を印可し、個別出力線より対象物の表面形状に応じて変化する電流Ｉを取り出せば良い。

【００１４】斯うした発明を具現化する静電容量検出素子の構造を図４を用いて説明する。静電容量検出素子の信号増幅素子を成す信号増幅用ＭＩＳ型薄膜半導体装置はソース領域とチャンネル形成領域とドレイン領域とを含む半導体膜とゲート絶縁膜とゲート電極とを不可欠な構成要件としている。図４の構成例では此の信号増幅用ＭＩＳ型薄膜半導体装置を第一層間絶縁膜が被って居る。信号増幅用ＭＩＳ型薄膜半導体装置のソース領域には第一配線が接続され、ドレイン電極には第二配線が接続される。第一配線と第二配線との間には第二層間絶縁膜が設けられ、第一配線と第二配線とを電気的に分離している。静電容量検出素子の信号検出素子を成す容量検出電極は信号増幅用ＭＩＳ型薄膜半導体装置のゲート電極に接続され、第二層間絶縁膜上に形成される。容量検出電極上は容量検出誘電体膜が被い、容量検出誘電体膜は静電容量検出装置の最表面に位置する。容量検出誘電体膜は静電容量検出装置の保護膜の役割も同時に演ずる。図４では容量検出電極は第二配線にて形成されているが、容量検出電極を第一配線にて形成しても良い。図４の構成にて容量検出電極を第一配線で形成すると、図４で容量検出誘電体膜と記載してある膜と第二層間絶縁膜とが実際の容量検出誘電体膜となる。又、第二配線を第一層間絶縁膜上に形成し、第一配線を第二層間絶縁膜上に形成する事で容量検出電極を第一配線にて作成する事も可能となる。

【００１５】上述の構成にて本願発明の信号増幅用ＭＩＳ型薄膜半導体装置が効果的に信号増幅の機能を果たす為には、信号増幅用ＭＩＳ型薄膜半導体装置のトランジスタ容量C_Tや信号検出素子の素子容量C_Dを適切に定めねばならない。次に此等の関係を図５を用いて説明する。

【００１６】まず、測定対処物の凸部が容量検出誘電体膜に接しており、対象物が電気的に接地されて居る状況を考える。具体的には静電容量検出装置を指紋センサとして用い、この静電容量検出装置表面に指紋の山が接している状態の検出を想定する。信号増幅用ＭＩＳ型薄膜半導体装置のゲート電極長をＬ（μｍ）、ゲート電極幅をＷ（μｍ）、ゲート絶縁膜の厚みをt_{ox}（μｍ）、ゲート絶縁膜の比誘電率をε_{ox}として信号増幅用ＭＩＳ型薄膜半導体装置のトランジスタ容量C_Tを

$C_T=\varepsilon_0\cdot\varepsilon_{ox}\cdot L\cdot W/t_{ox}$

と定義する。ここでε_0は真空の誘電率で有る。更に、容量検出電極の面積をＳ（μm^2）、容量検出誘電体膜の厚みをt_D（μｍ）、容量検出誘電体膜の比誘電率をε_Dとして信号検出素子の素子容量C_Dを

$C_D=\varepsilon_0\cdot\varepsilon_D\cdot S/t_D$

と定義する（ε_0は真空の誘電率）。対象物表面が素子容量C_Dの接地電極となり、容量検出電極が容量検出誘電体膜を挟んで他方の電極に相当する。容量検出電極は信号増幅用ＭＩＳ型薄膜半導体装置のゲート電極に接続されて居るので、トランジスタ容量C_Tを持コンデンサーと素子容量C_Dを持つコンデンサーとが直列に接続される事に成る。此等二つの直列コンデンサーに電圧V_{dd}が印可されるのである（図５Ａ）。印可電圧は静電容量に応じて分割されるから、この状態にて信号増幅用ＭＩＳ型薄膜半導体装置のゲート電極に掛かる電圧V_{GT}は

【００１７】

【数１】

$$V_{GT}=\frac{V_{dd}}{1+C_D/C_T}$$

となる。従って、素子容量C_Dがトランジスタ容量C_Tよりも十分に大きい時

【００１８】

【数２】

$$C_D>>C_T$$

には、ゲート電圧は

【００１９】

【数３】

$$V_{GT}\approx 0$$

と近似され、ゲート電極には殆ど電圧が掛からない。その結果、信号増幅用ＭＩＳ型薄膜半導体装置はオフ状態となり、電流Ｉは窮めて小さくなる。結局、指紋の山に相当する対象物の凸部が静電容量検出装置に接した時に信号増幅素子が殆ど電流を流さない為には、静電容量検出素子を構成するゲート電極長やゲート電極幅、ゲート絶縁膜材質、ゲート絶縁膜厚、容量検出電極面積、容量検出誘電体膜材質、容量検出誘電体膜厚などを、素子容量C_Dがトランジスタ容量C_Tよりも十分に大きくなる様に設定せねばならない訳で有る。一般に「十分に大き

い」とは１０倍程度の相違を意味する。換言すれば素子容量C_Dとトランジスタ容量C_Tとが

$C_D > 10 \times C_T$

との関係を満たせば良い。この場合、V_{GT}/V_{dd}は０．１程度以下となり薄膜半導体装置はオン状態には成り得ない。対象物の凸部を確実に検出するには、対象物の凸部が静電容量検出装置に接した時に、信号増幅用ＭＩＳ型薄膜半導体装置がオフ状態に成る事が重要である。従って電源電圧V_{dd}に正電源を用いる場合には信号増幅用ＭＩＳ型薄膜半導体装置として、ゲート電圧がゼロ近傍でドレイン電流が流れないエンハンスメント型（ノーマリーオフ型）Ｎ型トランジスタを用いるのが好ましい。より理想的には、伝達特性に於けるドレイン電流が最小値となるゲート電圧（最小ゲート電圧）をV_{min}として、この最小ゲート電圧が

$0 < V_{min} < 0.1 \times V_{dd}$

との関係を満たす様な信号増幅用Ｎ型ＭＩＳ薄膜半導体装置を使用する。反対に電源電圧V_{dd}に負電源を用いる場合には信号増幅用ＭＩＳ型薄膜半導体装置として、ゲート電圧がゼロ近傍でドレイン電流が流れないエンハンスメント型（ノーマリーオフ型）Ｐ型トランジスタを用いる。理想的には信号増幅用Ｐ型ＭＩＳ薄膜半導体装置の最小ゲート電圧V_{min}が

$0.1 \times V_{dd} < V_{min} < 0$

との関係を満たす信号増幅用Ｐ型ＭＩＳ薄膜半導体装置を使用する事である。斯うする事に依り対象物の凸部を、電流値Ｉが非常に小さいとの形態にて確実に検出し得るので有る。

【００２０】次に対象物が容量検出誘電体膜に接しずに対象物距離t_Aを以て容量検出誘電体膜から離れて居る状況を考える。即ち測定対処物の凹部が容量検出誘電体膜上に有り、更に対象物が電気的に接地されて居る状況で有る。具体的には静電容量検出装置を指紋センサとして用いた時に、静電容量検出装置表面に指紋の谷が来て居る状態の検出を想定する。先にも述べた様に、本発明の静電容量検出装置では容量検出誘電体膜が静電容量検出装置の最表面に位置するのが望ましい。この時の等価回路図を図５Ｂに示す。容量検出誘電体膜に対象物表面が接していないので、容量検出誘電体膜と対象物表面との間には空気を誘電体とした新たなコンデンサーが形成される。此を対象物容量C_Aと名付け、真空の誘電率ε_0と空気の比誘電率ε_Aと容量検出電極の面積Ｓとを用いて、

$C_A = \varepsilon_0 \cdot \varepsilon_A \cdot S / t_A$

と定義する。斯うして対象物が容量検出誘電体膜から離れた状態では、トランジスタ容量C_Tと素子容量C_Dと対象物容量C_Aとを持つ三つのコンデンサーが直列に接続され、此等三つのコンデンサーに電圧V_{dd}が印可される事になる（図５Ｂ）。印可電圧は静電容量に応じて三つのコンデンサー間で分割されるので、この状態にて

信号増幅用ＭＩＳ型薄膜半導体装置のゲート電極に掛かる電圧V_{GV}は

【００２１】

【数４】

$$V_{GV} = \frac{V_{dd}}{1 + \frac{1}{C_T} \cdot \left(\frac{1}{1/C_D + 1/C_A} \right)}$$

となる。一方、本発明では対象物が静電容量検出装置に接した時にドレイン電流が非常に小さくなる様に

【００２２】

【数５】

$$C_D >> C_T$$

との条件を満たすべく静電容量検出素子を作成して在るので、V_{GV}は更に

【００２３】

【数６】

$$V_{GV} \approx \frac{V_{dd}}{1 + C_A / C_T}$$

と近似される。結局、トランジスタ容量C_Tが対象物容量C_Aよりも十分に大きければ、

【００２４】

【数７】

$$C_T >> C_A$$

ゲート電圧V_{GV}は

【００２５】

【数８】

$$V_{GV} \approx V_{dd}$$

と、電源電圧V_{dd}に略等しくする事が可能と化す。この結果、信号増幅用ＭＩＳ型薄膜半導体装置をオン状態と出来、電流Ｉは窮めて大きくなる。指紋の谷に相当する対象物の凹部が静電容量検出装置上に来た時に信号増幅素子が大電流を通す為には、信号増幅素子を構成するゲート電極長やゲート電極幅、ゲート絶縁膜材質、ゲート絶縁膜厚などを、トランジスタ容量C_Tが対象物容量C_Aよりも十分に大きくなる様に構成付ける必要がある。先に述べた如く、１０倍程度の相違が認められると一般に十分に大きいと言えるので、トランジスタ容量C_Tと対象物容量C_Aとが

$C_T > 10 \times C_A$

との関係を満たせば良い。この場合、V_{GT}/V_{dd}は０．９１程度以上となり薄膜半導体装置は容易にオン状態と化す。対象物の凹部を確実に検出するには、対象物の凹部が静電容量検出装置に近づいた時に、信号増幅用ＭＩＳ型薄膜半導体装置がオン状態に成る事が重要である。電源電圧V_{dd}に正電源を用いる場合には信号増幅用ＭＩＳ型薄膜半導体装置としてエンハンスメント型（ノーマリーオフ型）Ｎ型トランジスタを用ており、このトランジスタの閾値電圧V_{th}がV_{GV}よりも小さい

のが好ましい。より理想的には、

$0 < V_{th} < 0.91 \times V_{dd}$

との関係を満たす様な信号増幅用N型ＭＩＳ薄膜半導体装置を使用する。反対に電源電圧V_{dd}に負電源を用いる場合には信号増幅用ＭＩＳ型薄膜半導体装置としてエンハンスメント型（ノーマリーオフ型）Ｐ型トランジスタを用いており、理想的には信号増幅用Ｐ型ＭＩＳ薄膜半導体装置の閾値電圧V_{th}がV_{GV}よりも大きいのが好ましい。より理想的には、

$0.91 \times V_{dd} < V_{th} < 0$

との関係を満たす信号増幅用Ｐ型ＭＩＳ薄膜半導体装置を使用する事である。斯うする事に依り対象物の凹部が、電流値Ｉが非常に大きいとの形態にて確実に検出されるに至る。

【００２６】結局、指紋の山等に相当する対象物の凸部が静電容量検出装置に接した時に信号増幅素子が殆ど電流を通さず、同時に指紋の谷等に相当する対象物の凹部が静電容量検出装置に近づいた時に信号増幅素子が大きな電流を通して対象物の凹凸を正しく認識するには、静電容量検出素子にて容量検出誘電体膜が静電容量検出装置の最表面に位置し、信号増幅用ＭＩＳ型薄膜半導体装置のゲート電極長Ｌ（μm）やゲート電極幅W（μm）、ゲート絶縁膜の厚みt_{ox}（μm）、ゲート絶縁膜の比誘電率ε_{ox}、容量検出電極面積Ｓ（μm^2）、容量検出誘電体膜の厚みt_D（μm）、容量検出誘電体膜の比誘電率ε_Dを素子容量C_Dがトランジスタ容量C_Tよりも十分に大きくなる様に設定する必要があり、且つ対象物が容量検出誘電体膜に接しずに対象物距離t_Aを以て離れて居る際にトランジスタ容量C_Tが対象物容量C_Aよりも十分に大く成る様に静電容量検出装置を構成づけるのが理想的と言える。より具体的には素子容量C_Dとトランジスタ容量C_Tと対象物容量C_Aとが

$C_D > 10 \times C_T > 100 \times C_A$

との関係を満たす様に静電容量検出装置を特徴付ける。又、電源電圧V_{dd}に正電源を用いる場合には信号増幅用ＭＩＳ型薄膜半導体装置としてエンハンスメント型（ノーマリーオフ型）N型トランジスタを用いるのが好まく、此のN型トランジスタの最小ゲート電圧は

$0 < V_{min} < 0.1 \times V_{dd}$

との関係を満たし、更に閾値電圧V_{th}がV_{GV}よりも小さく、具体的には

$0 < V_{th} < 0.91 \times V_{dd}$

との関係を満たしているエンハンスメント型N型トランジスタを用いるのが理想的である。反対に電源電圧V_{dd}に負電源を用いる場合には信号増幅用ＭＩＳ型薄膜半導体装置としてエンハンスメント型（ノーマリーオフ型）Ｐ型トランジスタを用いるのが好ましく、此のＰ型トランジスタの最小ゲート電圧V_{min}は

$0.1 \times V_{dd} < V_{min} < 0$

との関係を満たし、更に閾値電圧V_{th}がV_{GV}よりも大きく、具体的には

$0.91 \times V_{dd} < V_{th} < 0$

との関係を満たしているエンハンスメント型Ｐ型トランジスタを用いるのが理想的である。

【００２７】次に本発明に依る静電容量検出装置の全体構成を図６を用いて説明する。対象物の表面形状を読み取る静電容量検出装置はM行Ｎ列の行列状に配置されたM本（Mは１以上の整数）の個別電源線と、Ｎ本（Ｎは１以上の整数）の個別出力線、及び個別電源線と個別出力線との交点に設けられた静電容量検出素子とを最小限の構成要素としている。此等に加えて本発明に依る静電容量検出装置はM本の個別電源線に接続する電源選択回路や、Ｎ本の個別出力線に接続する出力信号選択回路のどちらか一方、或いは両者をも具備して居ても良い。静電容量検出素子は容量検出電極と容量検出誘電体膜と信号増幅素子とを含み、対象物との距離に応じて変化する静電容量を検出する。静電容量検出素子がM行Ｎ列の行列状に配置されているので、対象物の表面形状を読み取るには行と列とを其々順次走査してM×Ｎ個の静電容量検出素子を適当な順番に選択して行かねばならない。各静電容量検出素子に如何なる順序にて電源を供給して行くかを定めるのが電源選択回路である。電源選択回路は少なくとも共通電源線と電源用パスゲートとを含んで居り、M本の個別電源線の何れに電源供給するかを選択する。此とは対照的に各静電容量検出素子から如何なる順序にて検出された信号を読み出すかを定めるのが出力信号選択回路である。出力信号選択回路は少なくとも共通出力線と出力信号用パスゲートとを含んで居り、Ｎ本の個別出力線の何れから出力信号を取り出すかを選択する。

【００２８】静電容量検出素子内の信号増幅素子はゲート電極とゲート絶縁膜と半導体膜とから成る信号増幅用ＭＩＳ型薄膜半導体装置から構成される。又、電源用パスゲートもゲート電極とゲート絶縁膜と半導体膜とから成る電源パスゲート用ＭＩＳ型薄膜半導体装置から構成され、出力信号用パスゲートもゲート電極とゲート絶縁膜と半導体膜とから成る出力信号パスゲート用ＭＩＳ型薄膜半導体装置から成る。本願発明では信号増幅素子用ＭＩＳ型薄膜半導体装置のソース領域は個別出力線に接続され、信号増幅素子用ＭＩＳ型薄膜半導体装置のドレイン領域は個別電源線に接続され、信号増幅素子用ＭＩＳ型薄膜半導体装置のゲート電極は容量検出電極に接続される。（図６ではＭＩＳ型薄膜半導体装置のソース領域をＳ、ドレイン領域をＤ、ゲート電極をＧにて表示して居る。）斯うして個別電源線と個別出力線とは、容量検出電極にて検出された電荷Ｑに感応するチャンネル形成領域を介在してお互いに接続される。

【００２９】一方、電源パスゲート用ＭＩＳ型薄膜半導体装置のソース領域は個別電源線に接続され、電源パスゲート用ＭＩＳ型薄膜半導体装置のドレイン領域は共通

電源線に接続され、電源パスゲート用ＭＩＳ型薄膜半導体装置のゲート電極はM本の個別電源線の内からどの個別電源線を選択するかと云った信号を供給する電源選択用出力線に接続される。電源選択用出力線は一例として電源用シフトレジスタの各出力段となし得るし（図６の場合）、或いは電源用シフトレジスタに代わる電源用デコーダーの各出力段ともなし得る。電源用シフトレジスタはM個の出力段に転送されて来た選択信号を順次供給して行く。又、電源用デコーダーはデコーダーへの入力信号に応じてM個の出力段から特定の出力段を選定する。斯うしてM個の電源用パスゲートには順次選択信号が入力され、結果としてM本の個別電源線が共通電源線と順次電気的な導通が取られて行く。信号増幅素子用ＭＩＳ薄膜半導体装置のドレイン領域は個別電源線に接続しているので、選択された個別電源線に接続する信号増幅素子は一斉に対象物の表面形状に応じた電流を各個別出力線に供給する事に成る。

【００３０】本願発明では出力信号パスゲート用ＭＩＳ型薄膜半導体装置のソース領域は共通出力線に接続され、出力信号パスゲート用ＭＩＳ型薄膜半導体装置のドレイン領域は個別出力線に接続され、出力信号パスゲート用ＭＩＳ型薄膜半導体装置のゲート電極はN本の個別出力線の内からどの個別出力線を選択するかと云った信号を供給する出力選択用出力線に接続されて居る。出力選択用出力線は一例として出力信号用シフトレジスタの各出力段となし得るし（図６の場合）、或いは出力信号用シフトレジスタに代わる出力信号用デコーダーの各出力段ともなし得る。出力信号用シフトレジスタはN個の出力段に転送されて来た選択信号を順次供給して行く。又、出力信号用デコーダーはデコーダーへの入力信号に応じてM個の出力段から特定の出力段を選定する。斯うしてN個の出力信号用パスゲートには順次適時選択信号が入力され、結果としてN本の個別出力線が共通出力線と順次電気的な導通が取られて行く。信号増幅素子用ＭＩＳ型薄膜半導体装置のソース領域は個別出力線に接続しているので、電源選択回路にて選択された個別電源線に接続するN個の信号増幅素子の内で唯一出力信号選択回路にて選択された個別出力線に接続する信号増幅素子だけが、対象物の表面形状に応じた電流を共通出力線に供給する事に成る。以降同様にして、M本の個別出力線の内の一本が選択された状態にてN本の個別出力線を順次走査して行く事で、M行N列の行列状静電容量検出素子からの信号が順番に共通出力線に供給されて行くのである。

【００３１】斯うした構成にて静電容量検出装置が機能する為には、個別出力線と共通出力線と電源選択用出力線とが第一配線にて配線され、個別電源線と共通電源線と出力選択用出力線とが第二配線にて配線され、此等第一配線と該第二配線とは絶縁膜を介して電気的に分離される必要が有る。容量検出電極は第一配線にて配線されても良いし、或いは第二配線にて配線されても良い。斯うした構成を成す事で余分な配線を除去し、以て各配線間に生ずる寄生容量を最小化せしめ、故に微少な静電容量を高感度にて検出せしめる訳である。

【００３２】斯様な静電容量検出素子は前述の転写技術を用いて、プラスティック基板上に形成され得る。単結晶硅素技術に基づく指紋センサはプラスティック上では直ぐに割れてしまったり、或いは十分な大きさを有さぬが為に実用性に乏しい。これに対して本願発明に依るプラスティック基板上の静電容量検出素子は、プラスティック基板上で指を被うに十分に大きい面積としても静電容量検出素子が割れる心配もなく、プラスティック基板上での指紋センサとして利用し得る。具体的には本願発明により個人認証機能を兼ね備えたスマートカードが実現される。個人認証機能を備えたスマートカードはキャッシュカード(bankcard)やクレジットカード(credit card)、身分証明書(Identity card)等で使用され、此等のセキュリティーレベルを著しく高めた上で尚、個人指紋情報をカード外に流出させずに保護するとの優れた機能を有する。

【００３３】（実施例１）ガラス基板上に薄膜半導体装置からなる静電容量検出装置を製造した上で、此の静電容量検出装置を特開平１１－３１２８１１やS. Utsunomiya et. al. Society for Information Display p. 916 (2000)に開示された転写技術を用いてプラスティック基板上に転写し、プラスティック基板上に静電容量検出装置を作成した。静電容量検出装置は４００行４００列の行列状に並んだ静電容量検出素子から構成される。行列部の大きさは２０．３２mm角の正方形である。

【００３４】基板は厚み４００μmのポリエーテルスルフォン（ＰＥＳ）である。信号増幅用ＭＩＳ型薄膜半導体装置も出力信号パスゲート用ＭＩＳ型薄膜半導体装置も、電源パスゲート用ＭＩＳ型薄膜半導体装置も、出力信号用シフトレジスタを構成するＭＩＳ型薄膜半導体装置も、電源用シフトレジスタを構成するＭＩＳ型薄膜半導体装置も、総て同じ断面構造を有する薄膜トランジスタにて作られている。薄膜トランジスタは図４に示すトップゲート型で工程最高温度４２５℃の低温工程にて作成される。半導体膜はレーザー結晶化にて得られた多結晶硅素薄膜でその厚みは５９ｎｍである。又、ゲート絶縁膜は化学気相堆積法（ＣＶＤ法）にて形成された４８ｎｍ厚の酸化硅素膜で、ゲート電極は厚み４００ｎｍのタンタル薄膜から成る。ゲート絶縁膜を成す酸化硅素膜の比誘電率はＣＶ測定により略３．９と求められた。第一層間絶縁膜と第二層間絶縁膜は原料物質としてテトラエチルオーソシリケート（ＴＥＯＳ：Ｓｉ（OCH_2CH_3）$_4$）と酸素とを用いてＣＶＤ法にて形成した酸化硅素膜である。第一層間絶縁膜はゲート電極（本実施例では４００ｎｍ）よりも２０％程度以上厚く、第二層間絶縁膜よりも薄いのが望ましい。斯うするとゲート電極

を確実に覆って、ゲート電極と第一配線乃至は第二配線との短絡を防止し、同時に第二層間絶縁膜を厚くし得るからである。本実施例では第一層間絶縁膜を５００ｎｍとした。第二層間絶縁膜は第一配線と容量検出電極とを分離して居る。従って第一配線と容量検出電極との間に生ずる寄生容量を最小とし、好感度の静電容量検出装置を実現するには第二層間絶縁膜の誘電率は出来る限り小さく、その厚みは出来る限り厚い方が好ましい。而るにＣＶＤ法にて積層された酸化硅素膜の総厚みが２μｍ程度を越えると酸化膜に亀裂が生ずる場合があり、歩留まりの低下をもたらす。従って第一層間絶縁膜と第二層間絶縁膜との和は２μｍ程度以下とする。斯うする事で静電容量検出装置の生産性が向上する。先にも述べた様に第二層間絶縁膜は厚い方が好ましいので、第一層間絶縁膜よりも厚くする。第一層間絶縁膜はゲート電極よりも２０％程度以上厚く、第二層間絶縁膜は第一層間絶縁膜よりも厚く、第一層間絶縁膜と第二層間絶縁膜との和は２μｍ程度以下が理想的と言える。本実施例では第二層間絶縁膜の厚みを１μｍとした。第一配線と第二配線は何れも５００ｎｍ厚のアルミニウムより成り、配線幅は５μｍである。第一配線に依り電源選択用出力線と共通出力線、及び個別出力線が形成され、第二配線にて個別電源線と共通電源線、出力選択用出力線、及び容量検出電極が形成された。個別電源線と容量検出電極との間隔は５μｍで、個別出力線と容量検出電極との間隔も矢張り５μｍである。本実施例では静電容量検出装置を成す行列のピッチを５０．８μｍとし、解像度を５００ｄｐｉ（dots per inch）としている。従って容量検出電極は４０．８μｍ×４０．８μｍの大きさとなる。容量検出誘電体膜は厚み４００ｎｍの窒化硅素膜にて形成された。ＣＶ測定からこの窒化硅素膜の比誘電率は略７．５であったから、素子容量C_Dは凡そ２７６ｆＦ（フェムトファラッド）となる。本実施例の静電容量検出装置を指紋センサと想定すると、指紋の凹凸は４０μｍ程度なので、静電容量検出装置表面に指紋の谷が来た時の対象物容量C_Aは０．３６８ｆＦと計算される。一方、信号増幅用ＭＩＳ薄膜半導体装置のゲート電極長Ｌを４μｍとし、ゲート電極幅Ｗを５μｍとしたから、トランジスタ容量C_Tは凡そ１４．４ｆＦとなる。斯うして本実施例に示す静電容量検出素子は

$C_D > 10 \times C_T > 100 \times C_A$

との関係を満たす。斯くして電源電圧V_{dd}を３．３Ｖとすると、指紋の山が静電容量検出装置表面に接した時に信号増幅用ＭＩＳ薄膜半導体装置のゲート電極に印可される電圧V_{GT}は０．１６Ｖとなり、指紋の谷が来た時に此のゲート電極に印可される電圧V_{GV}は３．２２Ｖとなる。

【００３５】図７には本実施例にて用いたＭＩＳ型薄膜半導体装置の伝達特性を示す。出力信号用シフトレジスタと電源用シフトレジスタはＣＭＯＳ構成とされ、信号増幅用ＭＩＳ型薄膜半導体装置と電源パスゲート用ＭＩＳ型薄膜半導体装置、及び出力信号パスゲート用ＭＩＳ型薄膜半導体装置はＮＭＯＳトランジスタにて形成された。信号増幅用Ｎ型ＭＩＳ薄膜半導体装置の最小ゲート電圧V_{min}は０．１Ｖで有り、

$0 < V_{min} < 0.1 \times V_{dd} = 0.33V$

との関係を満たして居る。又、閾値電圧V_{th}は１．４７Ｖで、矢張り

$0 < V_{th} < 0.91 \times V_{dd} = 3.00V$

との関係を満たして居る。この結果、指紋の山が静電容量検出装置表面に接した時に信号増幅素子から出力される電流値は５．６×１０$^{-13}$Ａと窮めて微弱となる。反対に指紋の谷が来た時には信号増幅素子から２．４×１０$^{-5}$Ａと大きな電流が出力され、指紋等の凹凸情報を精度良く検出するに至った。

【００３６】

【発明の効果】以上詳述してきた様に、従来の単結晶硅素基板を用いた技術では数ｍｍ×数ｍｍ程度の小さな静電容量検出装置しかプラスティック基板上に形成出来なかったが、本願発明に依るとその百倍もの面積を有する静電容量検出装置をプラスティク基板上に作成する事が実現し、しかも対象物の凹凸情報を窮めて高精度に検出出来る様になった。その結果、例えはスマートカードのセキュリティーレベルを著しく向上せしめるとの効果が認められる。又、単結晶硅素基板を用いた従来の静電容量検出装置は装置面積の極一部しか単結晶硅素半導体を利用して居らず、莫大なエネルギーと労力とを無駄に費やしていた。これに対し本願発明では斯様な浪費を排除し、地球環境の保全に役立つとの効果を有する。

【図面の簡単な説明】

【図１】　従来技術に於ける動作原理を説明した図。

【図２】　本願発明に於ける動作原理を説明した図。

【図３】　本願発明に於ける動作原理を説明した図。

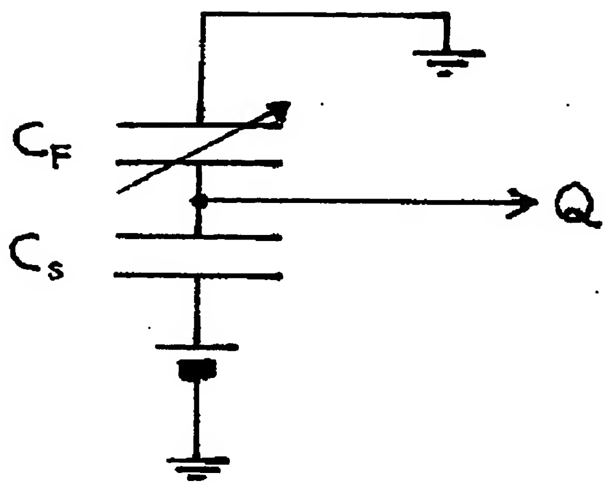
【図４】　本願発明の素子構造を説明した図。

【図５】　本願発明の原理を説明した図。

【図６】　本願発明全体構成を説明した図。

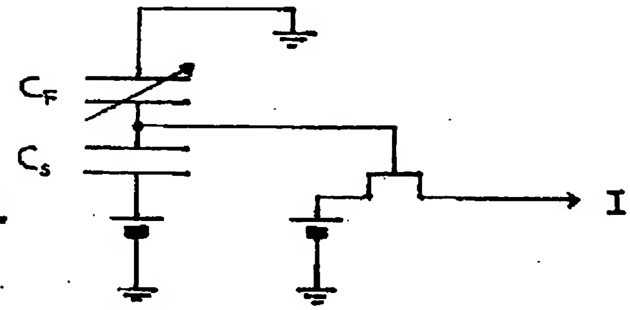
【図７】　本実施例にて用いた薄膜半導体装置の伝達特性図。

【図１】



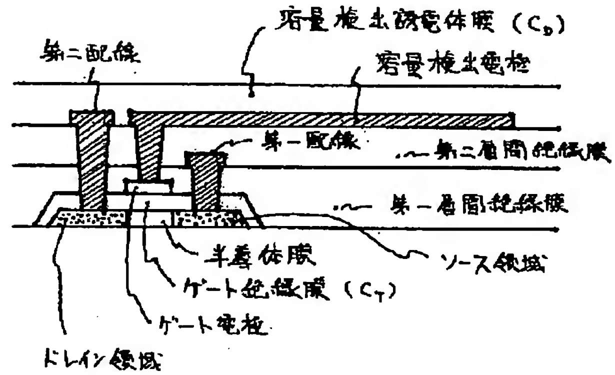
C_F
C_S
Q

【図２】



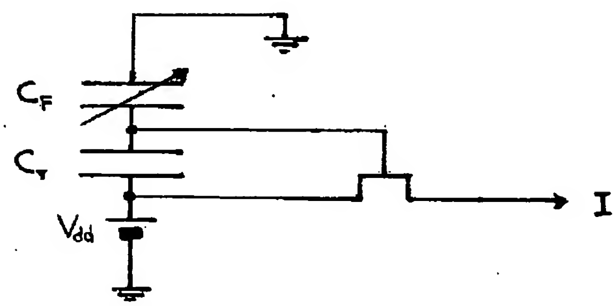
C_F
C_s
I

【図４】



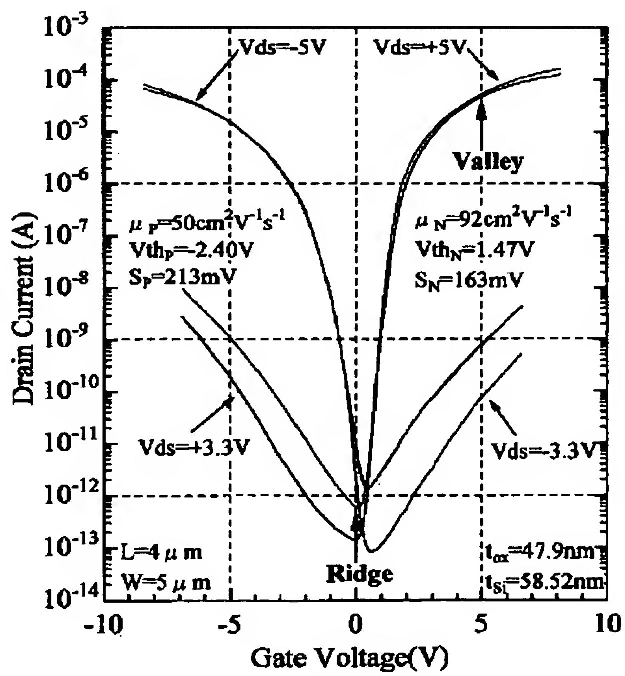
容量検出誘電体膜（C_D）
第二配線
容量検出電極
第一配線
第二層間絶縁膜
第一層間絶縁膜
半導体膜
ソース領域
ゲート絶縁膜（C_T）
ゲート電極
ドレイン領域

【図３】



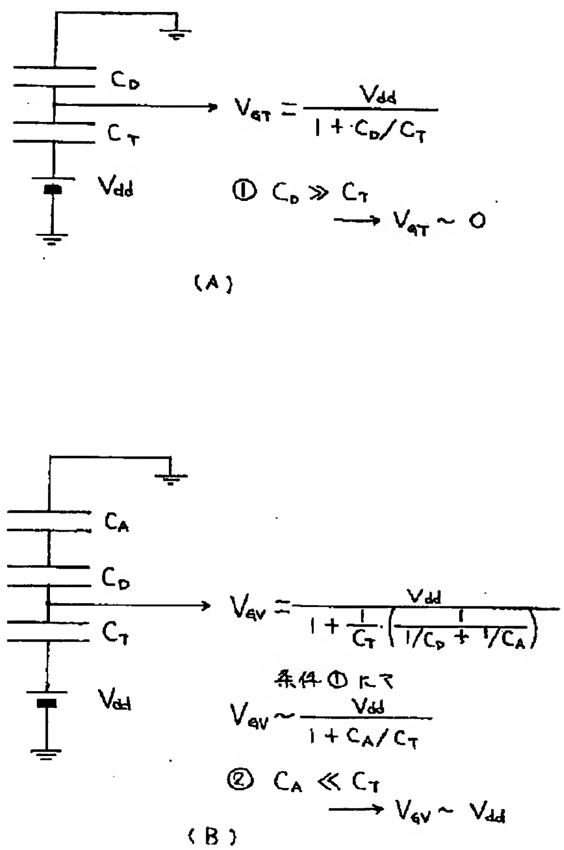
C_F
C_T
V_dd
I

【図７】

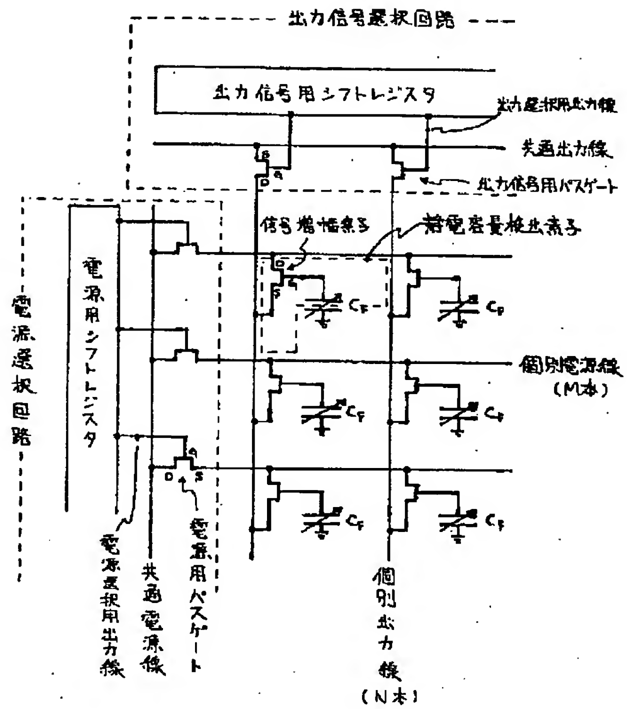


Vds=-5V
Vds=+5V
Valley
μ_P=50cm²V⁻¹s⁻¹
Vth_P=-2.40V
S_P=213mV
μ_N=92cm²V⁻¹s⁻¹
Vth_N=1.47V
S_N=163mV
Vds=+3.3V
Vds=-3.3V
L=4 μ m
W=5 μ m
Ridge
t_ox=47.9nm
t_Si=58.52nm
Drain Current (A)
Gate Voltage(V)
10^-3
10^-4
10^-5
10^-6
10^-7
10^-8
10^-9
10^-10
10^-11
10^-12
10^-13
10^-14
-10
-5
0
5
10

【図５】



【図６】



フロントページの続き

Ｆターム(参考)	2F063	AA43	BA29	BB02	BB08	BD05
		BD11	CA08	CA29	DA02	DA05
		DD07	HA04	LA11	LA30	
	4C038	FF01	FF05	FG00		
	5B047	AA25	AB02	BA02	BB10	BC01
	5F110	AA24	AA28	BB04	BB09	CC01
		DD01	EE04	FF02	FF29	GG02
		GG13	GG25	HL03	NN03	NN04
		NN23	NN35	NN72	PP03	